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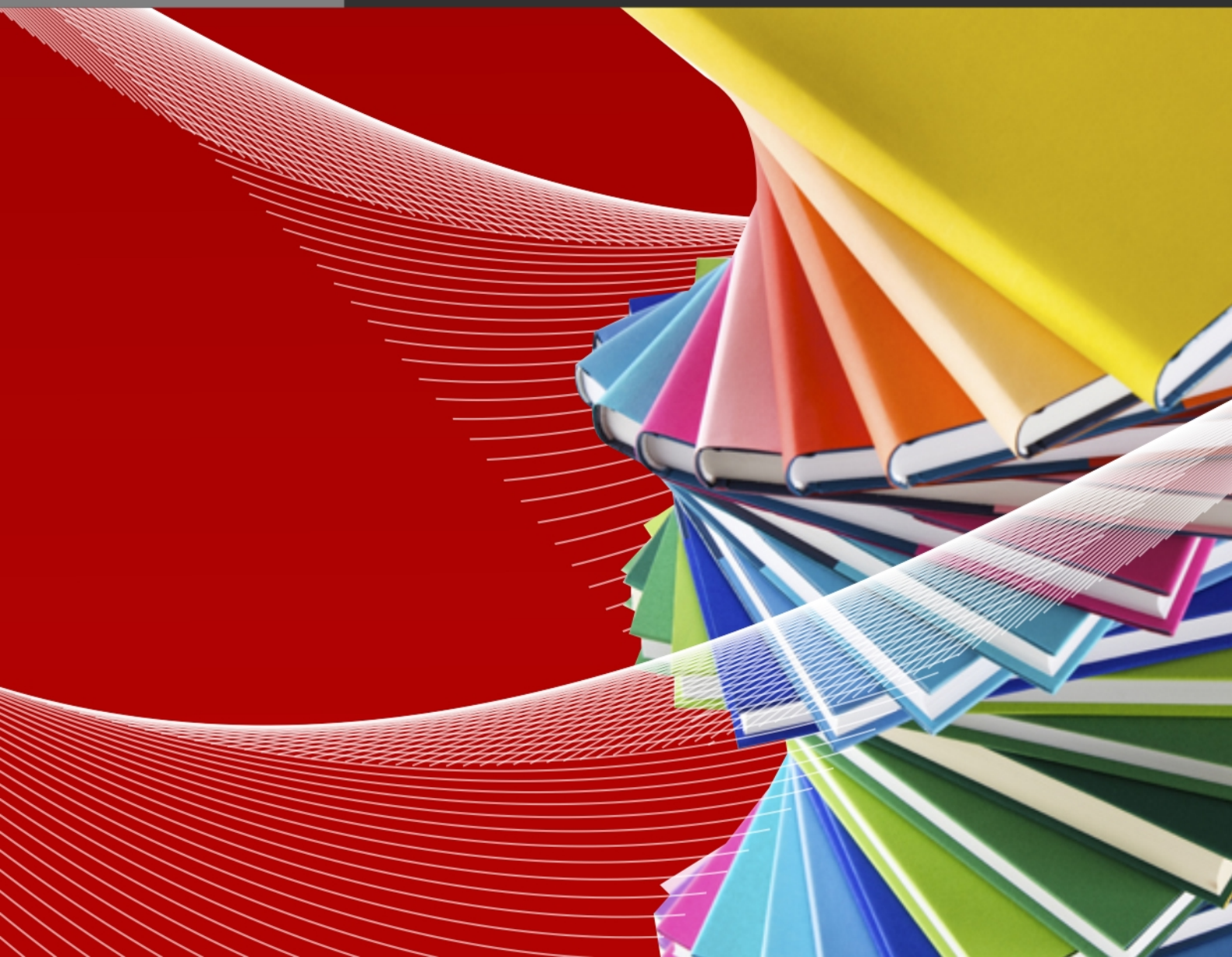

A 8-BIT 8GS/s HIERARCHICAL TIME-INTERLEAVED MULTI-BIT SAR ADC WITH DIGITAL CORRECTION

by

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Final Year Project Report submitted in partial fulfillment
of the requirements for the Degree of

Bachelor of Science in Electrical and Computer Engineering

2016

Faculty of Science and Technology
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This project report entitled "**A 8-BIT 8GS/s HIERARCHICAL TIME-INTERLEAVED MULTI-BIT SAR ADC WITH DIGITAL CORRECTION**" was prepared by ZHENG Zi Hao (D-B2-2858-2), WEI Lai (D-B2-2882-0), LIU Zi Yu (D-B2-875-1) in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical and Computer Engineering at the University of Macau.

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Signature : _____

Supervisor : Prof. Dr. ZHU Yan

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ABSTRACT

Due to the advanced noise-proof transmission characteristics of digital signal and the convenience brought digital signal processing, digital applications are expending exponentially. However, the world is analog, and the raw data and signals acquired for further processing or storage are analog as well. To perform digital process on those data and signals, analog-to-digital converters (ADC) are desired.

With the demand of high speed communication systems and high speed real-time control systems, such as broadband satellite communication systems, radar systems, broadband cable receivers and electronic back-end of optical cable receivers, high speed ADCs with moderate and/or conservative resolutions become a hot topic in ADC related research. In addition, low power consumption is a plus to the ADC to make it possible to be driven by batteries while maintain an acceptable battery life.

With all these considerations, successive approximation register (SAR) based ADCs stands out with the benefits of technology down scaling to achieve a high sampling rate in GHz range with moderate resolution (6-10 bits) and relatively low power consumption. Serval ADCs in this specification range are reported recently, such as [1] and [2] with advanced technology (32nm SOI and 28nm UTBB FDSOI)

In this project, an 8 GS/s 8 Bit Hierarchical Time-Interleaved Multi-Bit SAR ADC with Digital Error Correction is designed with 28nm standard CMOS technology. To achieve the target sampling rate, time-interleaving structure is used to relax time window of conversion, while bring extra challenges to sampling front-end. Time-interleaved sampling front-end with interleaving factor M requires M clock signals with precise phases to ensure a uniform sampling in between channels. And jitter of each clock phases should also be well controlled to guarantee sampling accuracy.

And without the advantage of SOI technology used by [1][2], desired sampling bandwidth could not be achieved by a simple NMOS sampling switch. With all these consideration, a hierarchical time-interleaved structure with channel selection enabled bootstrap sampling switch in master hierarchy is proposed. And a 55dB sampling SNDR is achieved.

Unlike the single bit logic circuit, two bit per cycle logic circuit needs two extra comparators to split the reference voltage interval. Therefore, the noise caused by the comparator will be tripled than before. In order to achieve the same SNDR performance, the resolution of comparator needs to be increased. Besides, the design targets at quite high speed, thus the time used for comparison is limited. Thence, the comparator used in this design is required to have high resolution as well as high speed. The architecture used in the design is a double tail comparator combined with a pre-amplifier having regeneration part. The double tail comparator has higher gain formed by the input pair MOSFET, and the different clock signals provide extra current paths to expand the amplification time, so the speed sensitivity over the input voltage difference and noise performance are improved. As for the pre-amplifier, due to the help of different clock signals, the requirements on gain and linearity are not that critical. The difference between the two input signals just needs to be magnified three or four times, in this way, the pre-amplifier uses the basic common mode amplifier architecture with not large size MOSFET, which can avoid the effect of kickback noise and loading effect as well. During the regeneration period, the output of the pre-amplifier (input of the comparator) will be reset to Vdd. Hence, the input pair of comparator will be in saturation state when the comparing signal comes. Another problem may affect the accuracy of the comparator is the common mode voltage variation. To solve this problem, the Vcm-based switching method is applied.

The designed ADC operates under quite high speed, the total conversion time is limited. Compared with the single bit circuit, the two bit per cycle logic circuit will save much time as the conversion cycles is halved. However, during each conversion cycle of the two bit per cycle logic, more than one capacitor will be charged or discharged, besides, at least one of those charging or discharging capacitors has opposite movement compared with the others. So, each capacitor will have effect on the settling of the other capacitors. In this way, the top plate voltage may differ from the expected one, and the input signal cannot converge to Vcm. To avoid the error brought by the incorrect settling voltage, the redundant conversion step is added to the original process. The settling error in the former step will be compensated by the latter to ensure the signal voltage will finally converge to Vcm. Considering the tradeoff of effectiveness and complexity, the DAC array increases from 128C to 148C (C is the unit capacitor), thus the logic circuit can tolerate 15% settling error. In terms of speed, the dynamic logic is used instead of static logic to achieve high speed and lower power consumption. The digital error correction method is applied to transform the none-binary code into binary. [3]

[1] Kull, L., et al., "22.1 A 90GS/s 8b 667mW 64× interleaved SAR ADC in 32nm digital SOI CMOS," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, vol., no., pp.378- 379, 9-13 Feb. 2014

[2] Le Tual, S., et al., "22.3 A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI technology," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, vol., no., pp.382-383, 9-13 Feb. 2014

[3] J. H. Tsai et al., "A 0.003 mm 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS With Digital Error Correction and Correlated-Reversed Switching," in IEEE Journal of Solid-State Circuits, vol. 50, no. 6, pp. 1382-1398, June 2015.

Table of Contents

Chapter1 Introduction

1.1 Background of Analog-to-Digital Converters

In the recent years due to dramatically improvement of electronic technology. The electronic devices can be seen almost anywhere in our daily life. At the most part of those electronic devices are utilized the digital signal processing (DSP). But one thing we need to pay attention is that actually we are living in a world where full of analog signals, for example, change of temperature, velocity of vehicle, signal of mobile phones. These kinds of signals have very useful information for our daily life and scientific reach. So we need to find a fast and accuracy way to collect analog signals and convert analog signals into digital signal for further process. The analog-to-digital converter (ADC) functions as a bridge between the analog and digital worlds. It is the first step of the DSP system. So the ADC is a very significant building block in electronic devices that convert signal into digital domain. Nowadays through the development of electronic technology, the demand of ADC have been more and more harsh. In the practical application, the ADC also developed different types to conform different kinds of industry demand. Some kinds of architecture can have high speed and some kinds can have high resolution, etc. But with the rise of intelligent, more and more sensors are need for every kind of electronic devices that means a high-speed, low-power, medium- to high-resolution ADC is highly demanded. We think this is the trend of ADC design. In this paper we mainly introduced a kind of high-speed low-resolution ADC.

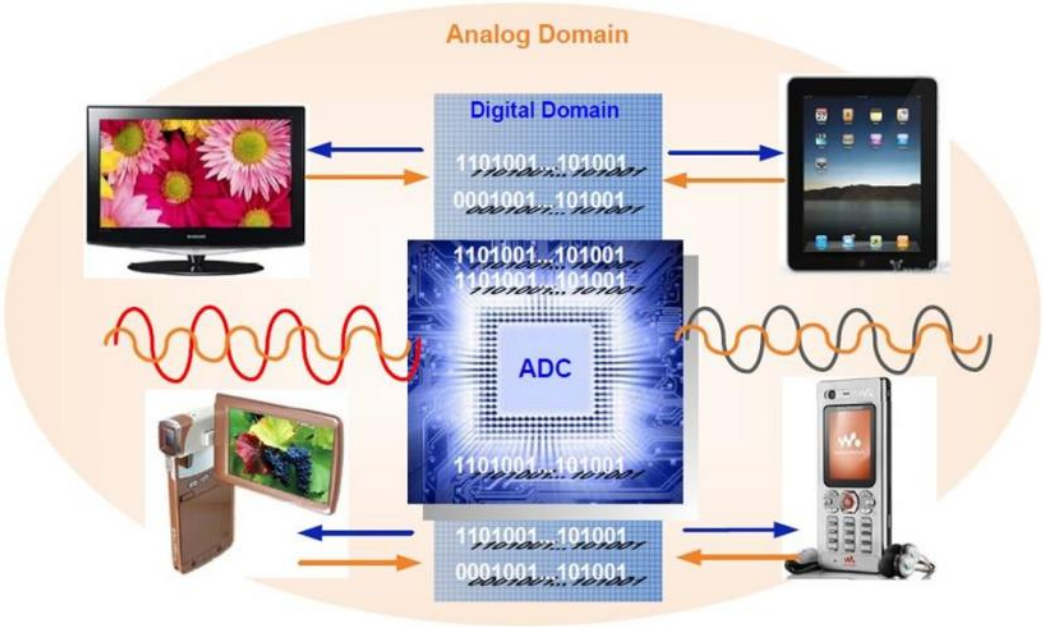

Figure 0.1 ADC as an interface between the analog and digital worlds

1.2 Application of ADC

ADC almost can be used in everywhere in human daily life. It is used so widely, for different function the ADCs architecture are also different. For different architectures, it can be roughly divide ADCs into Successive Approximation Register (SAR) ADC, Pipeline ADC, Flash ADC, etc. For different specification we can roughly divide ADCs based on speed, resolution and power consumption. It can be described as high-speed, low-resolution, low power consumption; high-speed, high-resolution, high power consumption, etc.

1.2.1 Radar Systems

The need for more digital signal processing is pushing the radar signal chain to transition to digital as early as possible, this trend let the ADC more and more close to the antenna side, which in turn introduces a number of challenging system-level considerations. To explore this further, Figure 1.2.1 illustrates a high level overview of a typical current X-band radar system. Within this system two analog mixing

stages are typically utilized. The first stage mixes the pulsed radar return to a frequency of around 1 GHz and the second to an IF in the region of 100 to 200 MHz to enable sampling of the signal using a 200 MSPS or lower A/D converter, to a resolution of 12 bits or higher. [1.1]

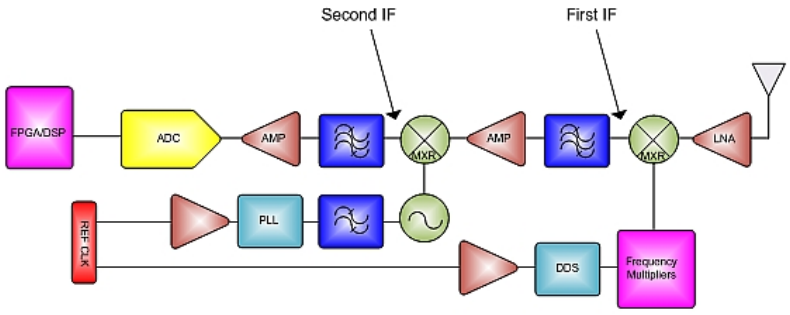

Figure 1.2.1 Example Radar Receiver Architecture Utilizing 1st and 2nd Ifs [1.1]

Within this architecture, aspects such as frequency agility and pulse compression may be implemented in the analog domain, which may require signal processing modifications and adjustments, but for the most part the system functionality is limited by the digitization rate.

In recent years gigasample per second (GSPS) ADCs have been pushing the transition to digital nearer to the antenna by moving the digitization point in the system to after the first mixing stage. Using a GSPS converter with an analog bandwidth in excess of 1.5 GHz already supports digitization of the first IF, but in many cases the performance of current GSPS ADCs has limited the acceptability of this solution as the linearity and noise spectral density of the device has not met the system requirements. In this thesis, the specification target an 8 bits, 8GS/s interleave front-end SAR ADC with two-bit per cycle logic. It can reach a relative high speed with a low resolution this chip maybe

1.2.2 Satellite broadband

Satellite broadband utilizes a Satellite to transmit the date and a receiver to receive the data. This type of Satellite broadband is the quickest to use. It allows both downloads and uploads to be done via the Satellite so high speeds can be used in both

directions and not just in 1 direction like in the 1 Way Satellite broadband. The block diagram is shown in Figure 1.2.2 satellite broadband block diagram.

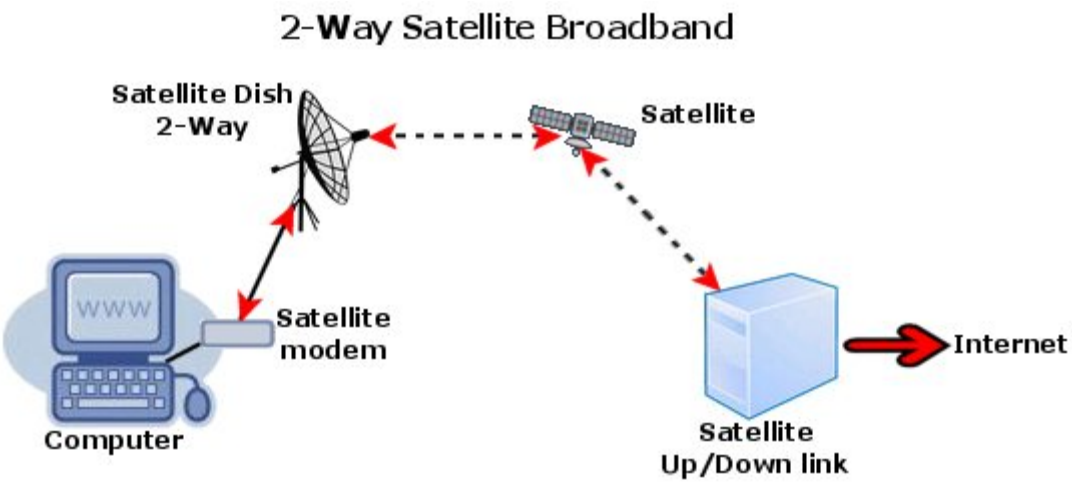

Figure 1.2.2 satellite broadband block diagram

From Figure 1.2.3 satellite work process block diagram we can see that the receptor need ADC to convert the received analog signal to digital signal for further step process. The satellite broadband communication system work in such a high frequency from 4GHz to 40GHz. Thus, the ADC should work fast enough to sample and convert the received signals into digital codes. So it definitely need a high speed ADC.

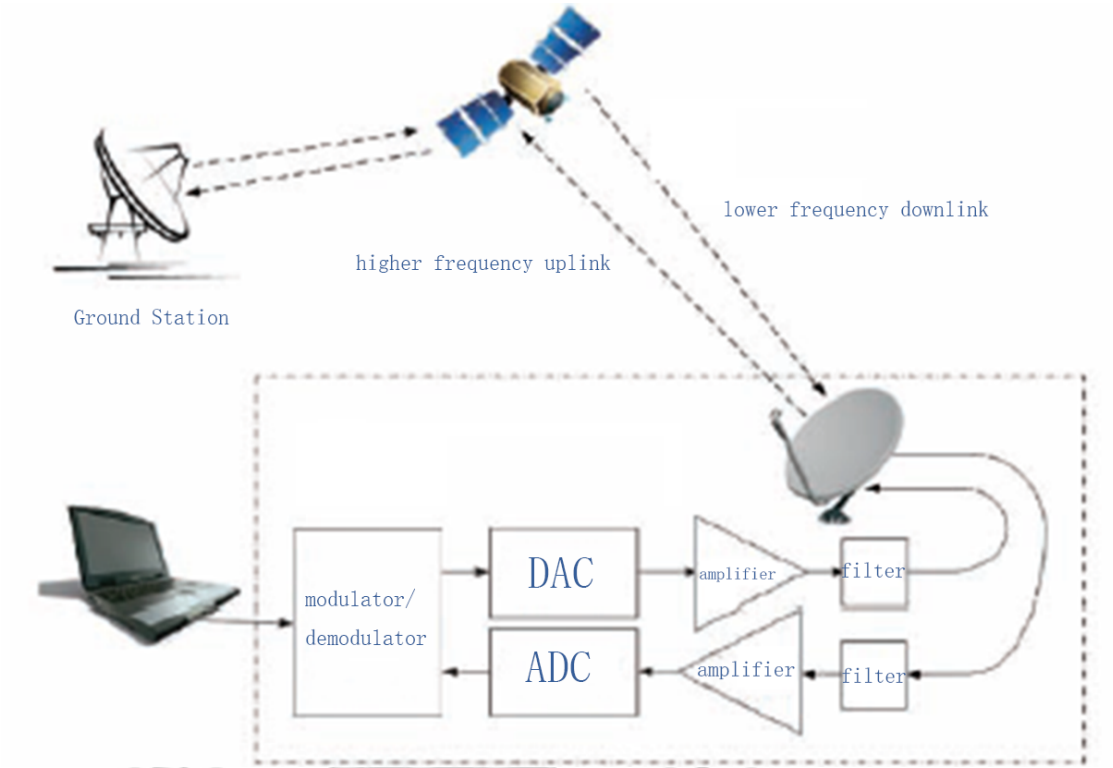

Figure 1.2.3 satellite work process block diagram

1.2.3 Cable receiver

Another use of high speed ADC is in cable receiver. For the modern world, the cable bandwidth already can reach to several hundred MHz, for example the upper edge of channel 83 in over-the-air television channels in the ultra-high frequency band, can reach to 890 MHz. In cable receiver, there is a block called Cable Downstream Processor (CDP) it will deal with the analog signal to digital. A typical cable receiver diagram with CDP is shown in the Figure 1.2.4 Cable receiver block diagram.

The CDP implements the physical interfaces and protocols required to provide the highest quality services of an in-band DOCSIS, EuroDOCSIS, DVB and OpenCable Set-Top Box (STB). The downstream signals are digitized by high speed ADC and passed to the Demod and Forward Error Correction (FEC) blocks, which do all the cable physical layer processing. This processing includes demodulating and Annex a (Europe), Annex B (US) or Annex C (Japan) FEC for the in-band data. The Out-Of Band (OOB) receiver consists of a QPSK demodulator with FEC, c, with

either internal MAC or POD support. Data are digitized by another high speed ADC. So a high speed ADC is necessary for the cable receiver.

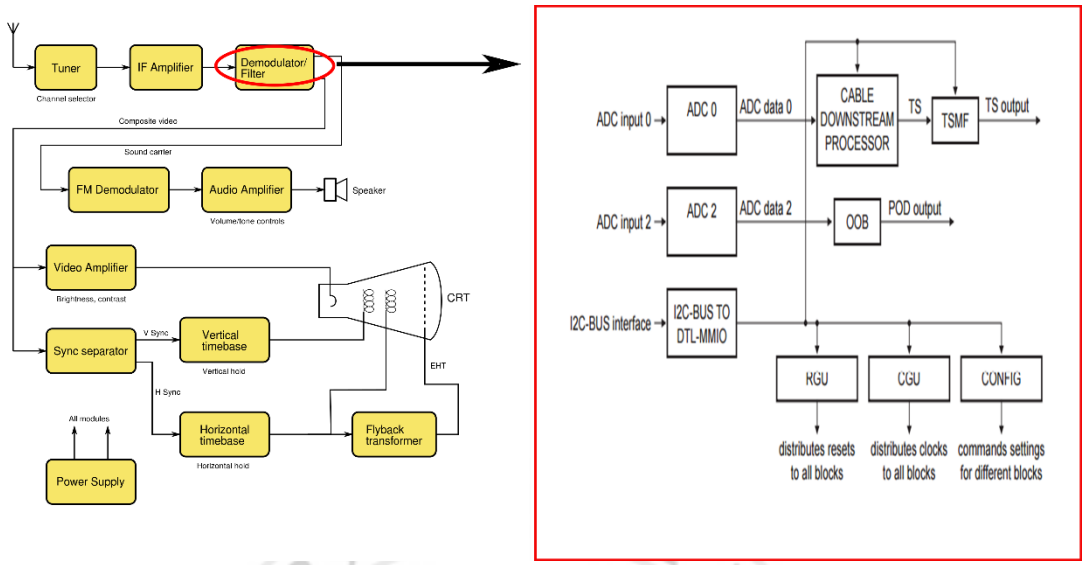

Figure 1.2.4 Cable receiver block diagram

1.3 Research Motivation

In this thesis, the target is to build an 8 bits 8 GHz ADC. As mentioned before, the ADC is used widely in our daily life. The high speed ADC can used in communication system. In order to improve the speed of ADC, there are a lot of different method. A very useful method is hierarchical time-interleaving front-end. Time-interleaving comes from a need based on limitations in available technologies, not only for speed, also for power- efficiency, because power-speed tradeoff in a single channel becomes nonlinear when conversion speed close to or reaches the limit of technology [1.2]. In this project, two essential considerations are achievable regeneration and settling time constants. These directly affect the dynamic performance of the converter (such as SFDR and sampling distortion) and limits the highest achievable sampling rate.

For a SAR ADC, critical requirements of regeneration and settling speed come from sampling front-end and also, comparator and SA operation on capacitive DAC. For a given comparator architecture and regeneration time constant, increasing the

regeneration time will decrease the error rate [1.3]. And a faster settling in SA operation on DAC will also help to reduce error rate in another way by decreasing the probability of inaccurate settling of residue that feed to the comparator. When reference error is counted in, the situation becomes more complex, but it will still benefit from a faster settling. In SAR architecture, at least N conversion cycle should be done to implement reference level search (usually binary, and could be non-binary with special consideration such as non-binary weighting redundant SA algorithm to implement digital error correction) required by SA algorithm. For a monolithic SAR ADC all these N conversion cycle should be done in its hold phase. And within each cycle both Target Specification comparator decision and DAC settling should be done. With the increase of sampling rate, it is very challenging to complete both process within narrowed hold time, especially for high resolution ADCs.

There are two mainstream prototypes of interleaved sampling front-end. The one is charge sharing structure and the other one is buffer structure. Hierarchical sampling front-end turns conventional flat structure into hierarchical structure with different levels. Two types of hierarchical sampling structures are reported in [1.4] [1.5] [1.6].

1.4 Organization of Thesis

The thesis is divided into five parts. **Chapter 1** gives a brief introduction of ADC and application of target specification ADC. It also specifies the motivation and the target specification of this project.

Chapter 2 gives a simple pre-analysis of the design considerations in ADC design. It analyzes the different parts of a SAR ADC and challenge in detail include harmonic distortion, thermal noise, bandwidth, clock feed-through, variation of on-resistance, timing mismatch and jitter. Also brief introduce the solution of those challenge: hierarchical technique, bootstrap circuit and redundancy technique.

Chapter 3 is dedicated to present the core of this thesis. It mainly include two part, the first part is hierarchical inter-leaved front-end. In this chapter, the different types of hierarchical interleaved front-end are introduced. The reason why the charge sharing type with Channel-Selection-Embedded (CSE) bootstrapped switch be chose

also conducted. Another part is two-bit per cycle SAR logic, also be introduced. The second important part of this chapter is two-bit per cycle SAR logic with redundancy. The two-bit per cycle SAR logic and interleaved front-end can improve the speed significantly. Hierarchy technique, CSE switch and redundancy are proposed to improve the performance of ADC.

Chapter 4 shows the circuit implementations of different components of the SAR ADC. And self-time loop also be shown to further help explain how the circuit work.

Chapter 5 shows the simulation result of the proposed circuit. And make analysis of result and generate power consumption diagram.

Chapter 6 finally draws the conclusion of this thesis and make a simple performance comparison with other ADC.

References

[1.1] Duncan Bosworth; "Demand for digital: Challenges and solutions for high-speed ADCs and RADAR systems," Analog Devices, June 11, 2014

[1.2]]Razavi, B., "Design Considerations for Interleaved ADCs," in *Solid-State Circuits, IEEE Journal of* , vol.48, no.8, pp.1806-1817, Aug. 2013

[1.3] Veendrick, Harry J.M., "The behaviour of flip-flops used as synchronizers and prediction of their failure rate," in *Solid-State Circuits, IEEE Journal of* , vol.15, no.2, pp.169-176, Apr 1980

[1.4] Kull, L., et al., "22.1 A 90GS/s 8b 667mW 64× interleaved SAR ADC in 32nm digital SOI CMOS," in *Solid-State Circuits*

Conference Digest of Technical Papers (ISSCC), 2014 IEEE International , vol., no., pp.378- 379, 9-13 Feb. 2014

[1.5] Le Tual, S., et al., "22.3 A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI technology," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International* , vol., no., pp.382-383, 9-13 Feb. 2014[1.6] El-Chammas, M.; Xiaopeng Li; Kimura, S.; Maclean, K.; Hu, J.; Weaver, M.; Gindlesperger, M.; Kaylor, S.; Payne, R.; Sestok, C.; Bright, W., "A 12 bit 1.6 GS/s BiCMOS 2×2 hierarchical time-interleaved pipeline ADC," in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2013 IEEE* , vol., no., pp.61-64, Sept. 30 2013-Oct. 3 2013

Chapter2 Pre-analysis

2.1 SAR Architecture

Due to the CMOS downscaling, a highly digitized ADC structure like SAR has become popular in recent years. As shown in Figure 2.1.1 [2.1], its simple architecture makes it achieve high speed and high resolution with low power consumption. It does not require active components like operational-amplifiers (op-amps) so that it does not consume static power. SAR ADC is composed of a comparator, a capacitive DAC, SAR logic and last but not the least, a sampling front-end for obtaining the input signal. A well-designed sampling front-end contributes little sampling distortions so as to enable a high-resolution design. Together with the increasing speed requirement, a traditional sampling front-end cannot sample the input signal with low sampling distortions. This is the first challenge for designing a high-speed, high-resolution ADC. For a high-resolution SAR ADC design, the comparator is required to compare a very little difference between the input signal and the reference. If the speed is high, the comparator will need to give out its decision in a really short time. Moreover, the comparator is required to suppress a certain level of noise for correct comparisons. The SAR logic is the spirit of this architecture, the logic performs binary search based on the decisions of the comparator. If the reference voltage is larger than the input signal, then “0” will be assigned to this bit. Otherwise, “1” will be assigned to this bit. According to the result, the SAR logic controls the switching of the DAC for generating a new reference level for the next comparison. In a high-speed high-resolution design, the logic delay is also one of the speed limitations that require special attention for the design. But for this project the speed is not such high, this problem can be ignored.

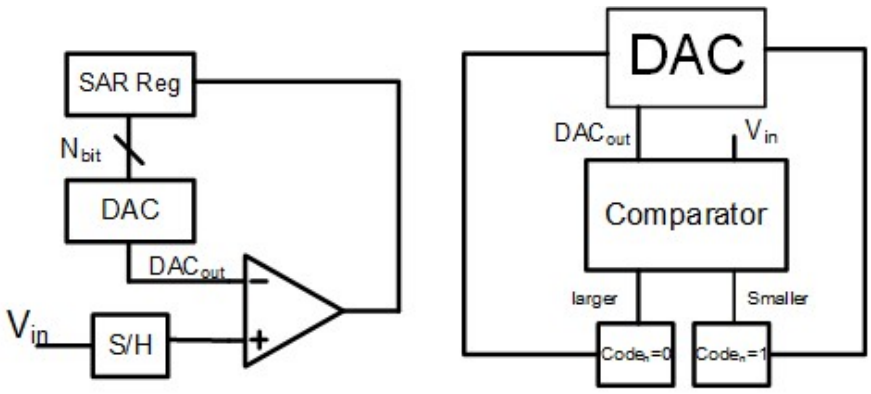

Figure 0.1.2 Architecture of a SAR ADC

Typical operation of a SAR ADC relies on the capacitive DAC to perform binary-searched feedback between the input signal and the reference voltage. In the sampling phase, the input signal is sampled to the DAC array through a sample-and-hold (S/H) circuit. During the conversion phase, first the comparator compares the input signal with the reference voltage. The first reference level is usually set as half of the input full scale. The comparator's decision is actually the output digital code, namely, "1" for larger input signal, "0" for larger reference voltage. This result is stored in the register starting from the MSB. Furthermore, the logic will change the reference level based on the comparator's result. If the comparator's result is "1", it means that the input signal is larger than the reference voltage, so the logic will change the reference level to a higher value by a factor of 2 for the next comparison. This procedure continues until the last bit is obtained.

2.1.1 Common-Mode Voltage Variation

The common-mode variation while using the advanced switching technique, should be discussed. As the DAC relies on the comparator to make the decision for each bit, the variation of common-mode voltage can affect the DC operating point of the comparator and ultimately degrade the conversion accuracy. One of the advantages of the V_{cm}-based switching is that the common-mode voltage is fixed while for the set-and-down switching, the common-mode voltage is varying from

V_{REF} to (5/8) V_{REF}. The common-mode voltage of the set-and-down approach is shown in Figure 2.1.2.

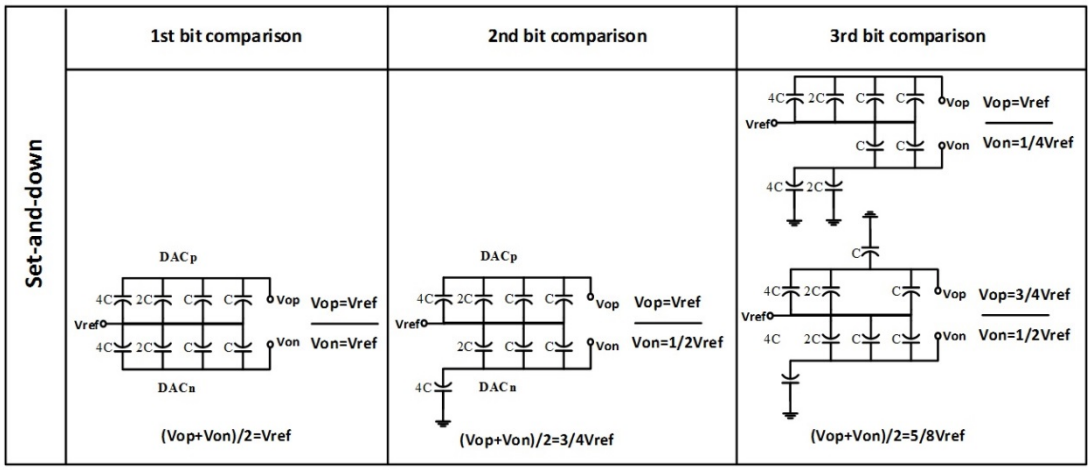

Figure 0.1.2 Common-mode voltage of the set-and-down switching

The common-mode voltage of the MSB comparison and the one of the LSB comparison may have a large difference. It will affect the DC operating point of the comparator and lead to a dynamic offset voltage during the conversion. However, for the V_{cm}-based method it does not have this variation problem, since the switching in the two DACs is differential. The common-mode voltage of the V_{cm}-based switching is always V_{cm}.

2.1.2 Dynamic Logic

For integrated circuit design, the concept of dynamic logic is distinguished from static logic by exploiting temporary storage of information in stray and gate capacitances. In the design of high speed ADC. Dynamic logic circuits are usually faster than static logic circuits, and require less surface area, but are more difficult to design. Compare with dynamic logic, the static logic implement by gate circuit which need more steps for logic calculation. The figure 2.1.3 shown a example of NAND dynamic logic.

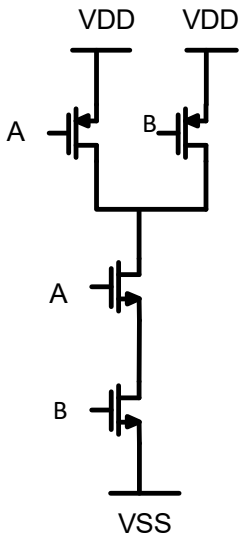

Figure 2.1.3 NAND Dynamic Logic

In this project, target speed is 8-GS/s, even used interleaved front-end. For the SAR logic part, each 2nd stage branch speed still have 1-GS/s. The implement of dynamic is shown in **Chapter 4.**

2.2 Sampling Front-end

2.2.1 Harmonic Distortion

Harmonic distortion is one of the main performance degradation in sampling network. Harmonics is introduced by the non-linear characteristics of realistic circuit component. For instance, the non-linear relationship of MOSFET on resistance and its drain to source voltage, gate to source voltage, and also, the dynamic change of threshold voltage of MOSFET due to the dynamic biasing when it is used as a sampling switch, especially for a large signal swing.

Total harmonic distortion (THD) is the merit of linearity of a network, which is defined as the ratio of the sum of the powers of all harmonic components to the power of the power of the fundamental in a certain frequency band. Normally, Signal-to-noise and distortion ratio (SNDR) is more usually used in the specification. SNDR is used to measure the linearity of the system.

$$SNDR_{dB} = SNR_{dB} + THD_{dB}$$

Since target specification of this ADC is 8Gs/s with 8X hierarchical time interleaving, 8-bit resolution with 1V supply in 28nm technology. According to ideal model, the upper limit of SNR should be 6.02*8+1.76=49.92 dB. To ensure a 53dB SNDR, the SNR target is set to 60dB. Thus for sampling front-end, SNDR target is set to be 53dB with thermal noise counted in for calculation.

2.2.2 Thermal Noise

DAC array is one of the most important components in the SAR ADC. By the different characteristics and operating principles, there are three DAC topologies, resistive type, capacitive type, and current-based type. In this thesis, capacitive type is used in DAC array for analog to digit conversion, the advantage of this type, firstly, is not require extra sample-and-hold (S/H) circuit. The capacitor itself has already have the S/H function. Secondly, capacitive type can effectively reduce the area of the circuit. Finally, capacitive type is also power efficiency compared with another two topologies. The total capacitance for the DAC array need to be set carefully, since it determines the fundamental thermal noise and also will influence the area of the ADC. The thermal noise is often limit the performance of an ADC design. In order to decide the value of the total capacitance, it is necessary to know the amount of thermal noise. For the design in this thesis, the targeted SNR is 56 dB, and noticing that the total noise is determined mainly by four main components: thermal noise, quantization noise, comparator noise and clock jitter. The expression for the total noise power is:

$$V_{noise}{}^2 = V_{kT/C}{}^2 + V_{quan}{}^2 + V_{comp}{}^2 + V_{CLK}{}^2$$

Where

$$V_{kT/C}{}^2 = \frac{2kT}{C}$$

$$V_{quan}{}^2 = \frac{\Delta^2}{12}$$

Where Δ is the scale of LSB. Notice that the thermal noise is doubled because the differential operation is adopted and the thermal noise in each part is uncorrelated. The T/H circuit can be modeled as a RC low-pass network. Total thermal noise power of the network can be calculated through integration of noise power spectral over frequency of this network, and can be expressed as $P=kT/Cs$, where Cs is sampling capacitance. SNR target is set to be 56dB, and SFDR target is set to be 60dB. As the differential input swing is set to be 1 $V_{p\text{-}p}$, single-ended signal swing for P channel or N channel is 0.5Vp-p. Total input power is P_{in} = (0.5V/2) ^{2}/2) = 0.125W, thus total noise power could be calculated with target SNR, it should be less than 0.125μW/Hz. The accumulated noise power at each capacitor arrays in sub ADCs, marked as N_{ch} is equal to 0.125μV^2/Hz. Since N_{ch} is contributed by the total 2 sets of capacitive DAC arrays required by two-bit per cycle control logic, noise power of each DAC array, marked as N_{array} could be calculated through the equation

$0.314\mu V^2/Hz/Hz > N_{ch}$ 4* N_{array}

Therefore, the noise power of each DAC capacitor array is

$N_{array}=N_{ch} / 2 = 0.0785\mu V^2/Hz/Hz=K_BT/C_{array}$

C_{array} =52.74fF

2.2.3 Bandwidth

The sampling network can be simplified as a RC network or a low pass filter. It can be realized by an equivalent model of a MOSFET when it is operating in the active mode. The equivalent resistance of a MOSFET and the sampling capacitance constitute a RC network as shown in Figure 2.2.1.

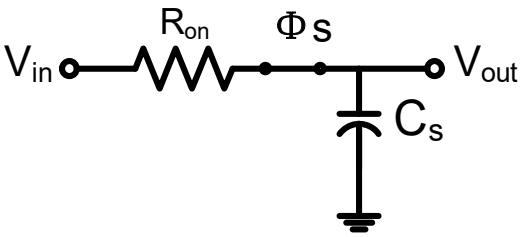

Figure 0.2.1 simplified of the resistance model of a MOSFET

The sampling frequency of this design is 8 GS/s, which is approximately 125ps per cycle. Considering the sizes of the switches and the conversion time required by the DAC array and the comparator, in this case, the sampling time was set as 125 ps. In order to provide sufficient time for the input signal to settle within 1 LSB, it is sufficient for the sampling time to be designed 10 times of the RC time constant of the sampling network:

$$T_s \approx 10\tau = 10RC$$

Where τ is the time constant for a RC circuit. The RC circuit stand of the MOSFET on-resistance and the total capacitance of the DAC array. The total capacitance C can be determined by thermal noise and the resolution specification. The settling time of the RC network consisted by sampling switch and sampling capacitor must be smaller than track phase. For master and slave T/H, t_{s_M} is 115ps and t_{s_S} is also 115ps. So, required on resistance of sampling switch could be calculated through

$$\tau = R_{on}C_s < 12.5ps$$

The result is Ron = 100Ω.

2.2.4 Clock Feed-through

Moreover, the clock feed-through effect also causes the sampling distortion. Figure 2.2.3 depicts the physical appearances of the overlap capacitances. The overlap capacitance is one of the contributions of C_{gs} and C_{gd}, as there is a small overlapping area between source and gate, and drain and gate, respectively. The clock signal at the gate will make its way through the drain via the overlap capacitance C_{ov}. The clock feed-through effect is measured as:

$$\Delta V_o = -\frac{C_{ov}}{C_{ov} + C_s}(V_{in} + V_{th} - V_L)$$

Where V_L is the clock voltage when it is low. The equation also shows that it is signal-dependent due to V_{in}.

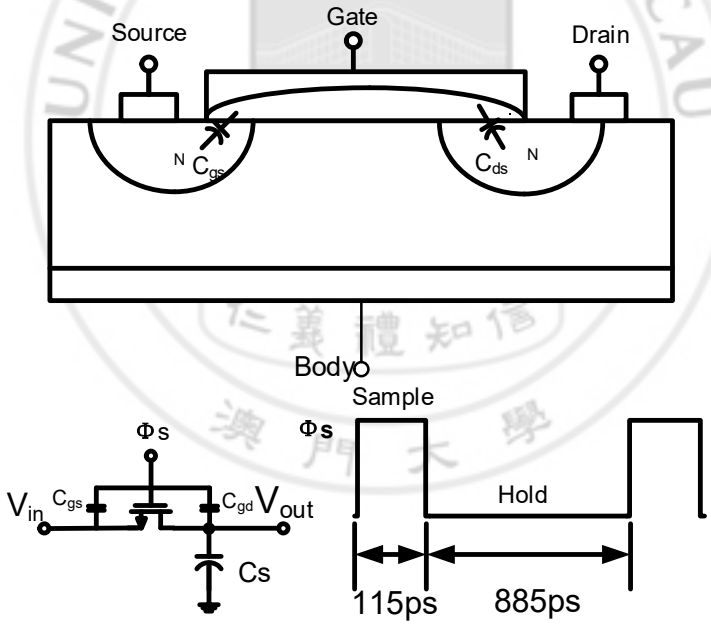

Figure 0.2.2 a diagram illustrating the clock feed-through

2.2.5 Variation of on-Resistance

In this design process the MOSFET is used as switch, the MOSFET is operating in triode region when switch is on and in the cut-off region when switch is off. When

switch is turned on, the MOSFET works in triode region, the on-resistance can be represented as:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})}$$

The V_{GS} variance with the variation of the input signal, therefore, the on-resistance also will vary with the change of V_{GS}. The on-resistance and the sampling capacitor can be seen as a low-pass filter, if the on-resistance varied, the sampling bandwidth will also have variance. Then, varying on-resistance causes sampling distortion.

2.2.6 Solution: Bootstrapped Sampling Switch

To avoid the variation of the on-resistance, bootstrap circuit is adopted to improve the sampling linearity. The idea of the bootstrapped switch is to provide a constant V_{gs} while it is sampling. When it is sampling, CLKs is high, so that switches is on. The gate voltage is $V_{DD}+V_{in}$ while the source voltage is V_{in}, therefore, V_{gs} is a constant V_{DD}. During the hold phase, CLksb causes switch is off. The solution provides a level shift of V_{in} that can produce a constant V_{GS} to the sampling switch. Therefore, the on-resistance remains constant during the tracking phase.

Figure 2.2.3 shows the sampling network with the use of a bootstrapped switch. It operates on a single phase clock that turns the switch M10 on and off. During the off phase, CLK is low. Devices M7 and M8 discharge the gate of M10 to ground. At the same time, is applied across capacitor Csp by M1 and M3. This capacitor will act as the battery across the gate and source during the “on” phase. M5 and M9 isolate the switch from Csp while it is charging. When CLK goes high, M2 pulls down the gate of M5, allowing charge from the battery capacitor Csp to flow onto gate G. This turns on both M9 and M10. M9 enables gate G to track the input voltage S shifted by, keeping the gate-source voltage constant regardless of the input signal. For example, if the source S is at V_{dd}, then gate G is at $2V_{dd}$; However $V_{gs}=V_{dd}$, because the body (n-well) of M5 is tied to its source, latch-up is suppressed.

Csp must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to

$$Vg = Vs + \frac{Csp}{Csp + Csp}$$

Where *Cp* is the total parasitic capacitance connected to the top plate of Csp while it is across the main switching device M10. When the switch is on, its gate voltage is greater than the analog input signal by a fixed difference of V_{dd}. This ensures that the switch is operated in a manner consistent with the reliability constraints. Because the switch is relatively independent of the signal, rail-to-rail signals can be used, which is important in minimizing power consumption. The switch linearity is also improved, and signal-dependent charge injection is reduced. Variations in on-resistance due to body effect, however, cannot be eliminated. [2.2]

Notice that the on-resistance affects the sampling bandwidth, as discussed above.

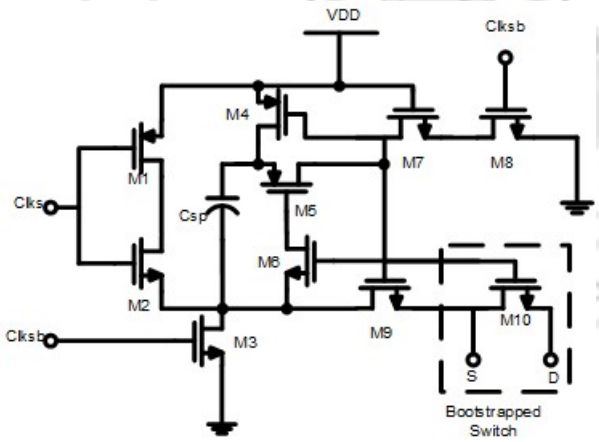

Figure 0.2.3 Bootstrapped sampling network

2.2.7 Timing Mismatch & Jitter

The performance of interleaved ADCs is ultimately limited by mismatches among the channels. Gain, offset, and timing mismatches heavily impact the overall signal-to-(noise + distortion) ratio (SNDR) at resolutions of 8 bits. The timing mismatch is the

most difficult to calibrate because it does not easily lend itself to detection or correction. [2.3]IT front-end need several clocks working at same time in series. The mismatch of different sampling clock is called phase error. Which means timing mismatch of each channel. That will decrease SNDR of IT front-end.

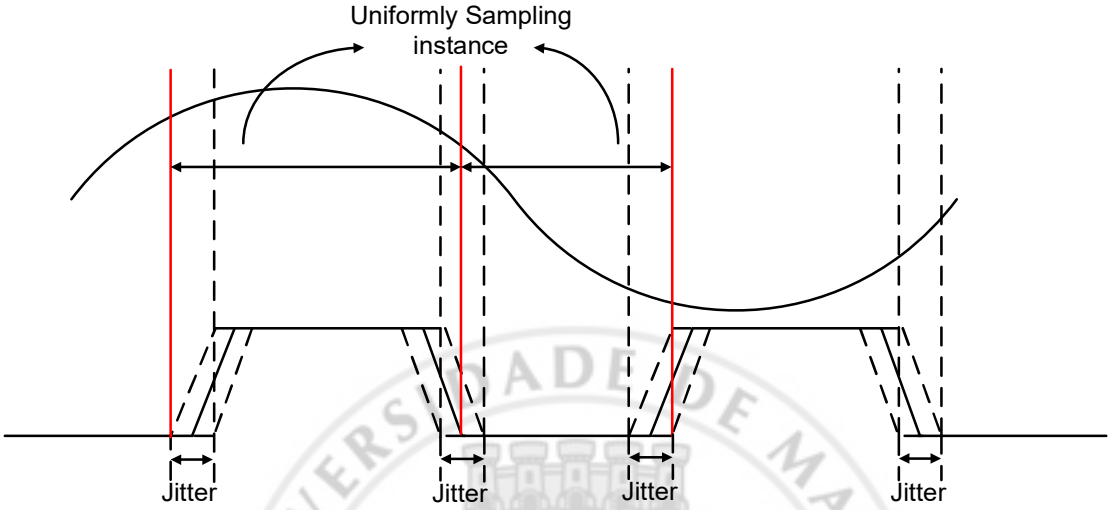

Figure 2.2.4 Jitter problem

Figure 2.2.4 shows an example of another problem -- jitter. Jitter is the phenomena that the rising edge and falling edge of sampling pulse variance in a small range. That variance will lead to the variance of interval of each sampling point which called uniformly sampling instance.

The conventional way to solve timing mismatch and jitter problem were using critical clock for each branch or add extra calibration circuit. Both of those means will consume large amount of power.

2.2.8 Solution: Hierarchical front-end

In this project, there proposed two measures to solve this problem: hierarchical time-interleaved front-end and channel-selection-embedded (CSE) bootstrapped sampling switch. T/H hierarchy allows to connect many ADC units to a single T/H. This approach makes it simpler to drive signal and clock at higher frequencies, but at the cost of shifting the problem of noise and nonlinearity in the T/H, due to the requirement for an additional sampling phase.[2.4] The amount of critical clocks can

be reduced significantly. For a two stage hierarchical time-interleaved front-end. Only first stage clock need to be set crucially. The second stage just sampling from DC voltage, so the clock can be relaxed. The Figure 2.2.5 shows an example of hierarchical IT sampling process.

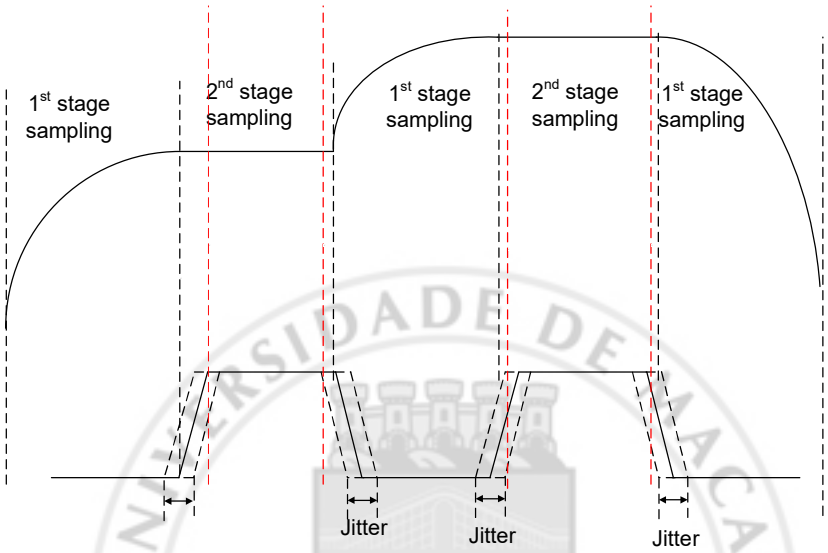

Figure 2.2.5 Sampling process

The proposed CSE-bootstrap circuit which can minimizes the master clock path to the bootstrap terminal by simply performing the channel selection in the bootstrap itself. That synchronizes the sampling instances of n TI-channels with a full speed master clock.[2.5] The detail of hierarchical TI front-end and CSE-bootstrap circuit will be shown in next chapter.

2.3 Comparator

2.3.1 Introduction

Comparator is one of the most important part in ADC design, which compares the input difference and outputs the logic signal “0” and “1” to the SAR controller for further logic processing. The comparator actually has same architecture with

amplifier but works in unstable station. This section mainly discussed the characteristics, metrics of the comparator. And introduce the comparator used in the project.

2.3.2 Characteristic

The circuit symbol of a comparator is shown in Figure 2.3.1, which has two analog input, V_{IP} and V_{IN}, and a digital output V_{OUT}. The ideal voltage transfer curve, V_{IP}-V_{IN} versus V_{OUT}, is shown in Figure 2.3.2. If the positive terminal V_{IP} has a larger voltage potential than the negative terminal V_{IN}, the output of the comparator V_{OUT} will output a logic "1", whereas if V_{IP} is less than V_{IN}, V_{OUT} will be "0". If V_{IP}=V_{IN}, the output will be undefined in an ideal comparator. So each comparator has a minimum resolution. When the comparator need higher resolution that means it will burn more power. It's a trade of in the design process need to consider for energy saving.

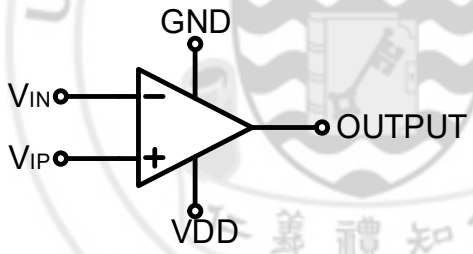

Figure 0.3.1Circuit symbol of a comparator

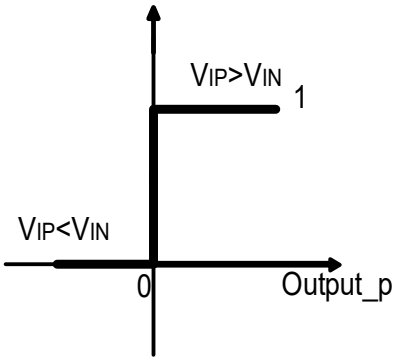

Figure 0.3.2 Ideal voltage transfer curve of a comparator

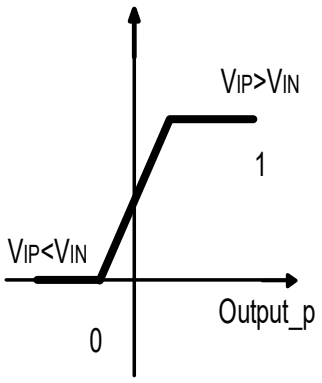

Figure 0.3.3 Practical voltage transfer curve of a comparator

The real case transfer curve of a comparator is shown in Figure 2.3.3 Outside the V_{IL} and V_{IH}, V_{OUT} will output "0" when $V_{IP}<V_{IN}$ and output "1" for $V_{IP}>V_{IN}$. However, if the input difference is quite smaller than resolution, the output cannot output a well-defined "0" or "1" within certain comparison time, since a real comparator has a finite gain. This situation is called "Metastability" in the comparator. In this project, front-end interleaving can reduces the metastability rate. Since each channel is given a longer time for conversion, the probability of metastability drops exponentially. [2.3]

2.3.3 Performance Metric

In the IC design process, comparator is a relative independent part in an ADC, the overall performance of the ADC could be limited if the comparator not fulfill the requirement. For design consideration, it is necessary to consider several performance metrics of the comparator which are listed as follow.

1) Gain

It is defined by Gain=$g_m t/C$,

Where g_m is the transconductance of the input transistors, t is the time for the input transistors operate in saturation region [2.6] [2.7] (also called as time of amplification) and C is the capacitive load.

For the same input difference, a comparator with higher gain can achieve higher resolution and SNR because it can expand the difference and suppress the noise more.

2) Conversion speed

Conversion speed is mainly dominated by time delay t_{delay} of the comparator. t_{delay} is the interval between the falling edge of reset phase and the rising edge of output. The equation of t_{delay} is expressed by

$$t_{delay} \approx \frac{C}{g_m} ln(\frac{V_o}{A_v \cdot V_{in}})$$

Where C is the capacitive of load, g_m is the transconductance of input transistors, V_{in} is the input signal, V_o is the output voltage, A_v is the gain of a preamplifier since the input signal will be amplified before the decision.

t_{delay} is inversely proportional to the scale of the input V_{IN}, i.e., a larger t_{delay} will be occurred if the input is smaller. Obviously, t_{delay} should be within the phase of decision, otherwise comparator cannot regenerate an exact "0/1" in time. In the project, due to using of two-bits per cycle and three comparators, the speed of comparator need to do comparison one time can be set as 68ps. excluding the sampling time and reserved time for logic delays, so 380 ps for reset and regeneration is allocated for the comparator. Figure 2.3.4 shown the clock diagram.

For the characteristic of comparator proposed in this project, the comparator have a pre-amplifier itself. That controlled by strobe1 and strobe2 is the real comparator clock.

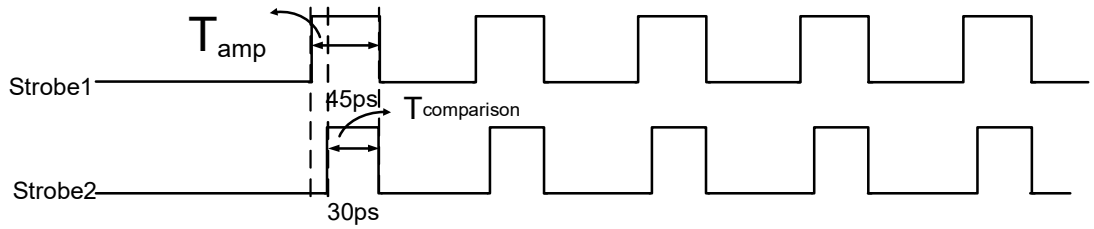

Figure 2.3.4 a clock diagram of the proposed comparator

3) Resolution

As shown in Figure 2.3.5, the resolution is defined as the minimum input voltage difference (V_{IN_min}) so that the comparator can output a well-defined logic level.

Assume V_{IN} is equal to V_{IN_min}, t_{delay_max} should be the allowed maximum time for delay. Once the delay is over t_{delay_max}, the comparator is failed to regenerate the digital output "0/1". In this project the resolution is 1/2 LSB. The full scale voltage is 0.7V, then the resolution is

V_{IN_min} =0.7/2^8*0.5=1.3mV

$$\text{Comparator SNDR} = 10\log\frac{P_{signal}}{P_{comparator\ noise}} = 56$$

Due to there have three comparators in the proposed architecture so the noise tripled. The SNDR of comparator shown above in order to get a better performance the resolution of comparator is set as 500 uV.

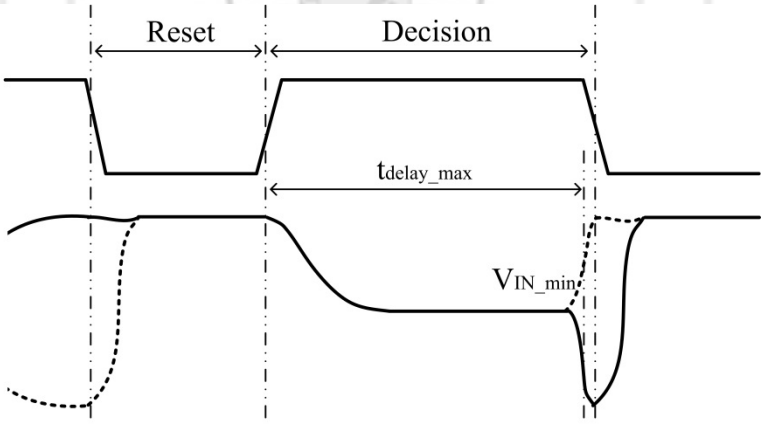

Figure 2.3.5 Resolution of a comparator

4) Intrinsic Offset

It is a certain input-referred voltage difference as Figure 2.3.6 shown, that causes by the mismatch of components. Comparing with the ideal transfer curve, the offset in the comparator causes a horizontal voltage shift V_{OS} of the ideal transfer curve as

shown in Figure 2.3.7. Hence, V_{OUT} will output "0" and "1" according to V_{IP}-V_{IN}<V_{OS} and V_{IP}-V_{IN}>V_{OS}, respectively.

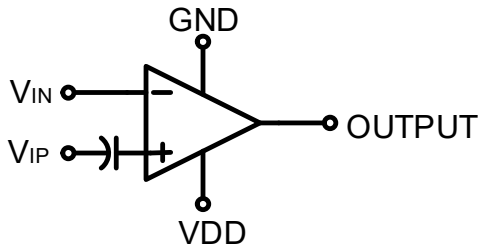

Figure 2.3.6 Comparator with offset modeling

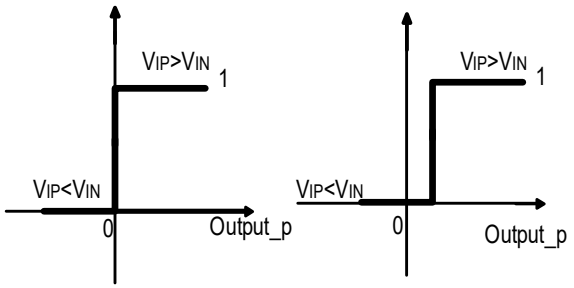

Figure 2.3.7 Ideal transfer curve and transfer curve with offset

2.3.4 Architecture of Comparator Design

The first considerations of the comparators should be the conversion speed, resolution and comparator noise. Although we targeted to design an 8 GS/s 53 dB SNDR SAR ADC in this project, moreover in fact, there not need to design such a high speed comparator. In the project, due to using of two-bits per cycle and three comparators, the speed of comparator need to do comparison one time can be set as 68ps. excluding the sampling time and reserved time for logic delays, so 380 ps for reset and regeneration is allocated for the comparator. On the other hand, considering the noise effect, the resolution of comparator should be targeted as 1.3mV.

Latch circuit is applied to this project as the Figure 2.3.8 shown in order to save the comparison result. This is to prove switch no change during capacitors charging and discharging process.

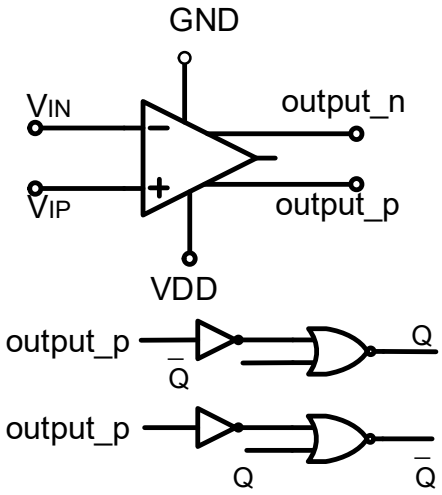

Figure 2.3.8 Block diagram of a comparator and corresponding latch circuit.

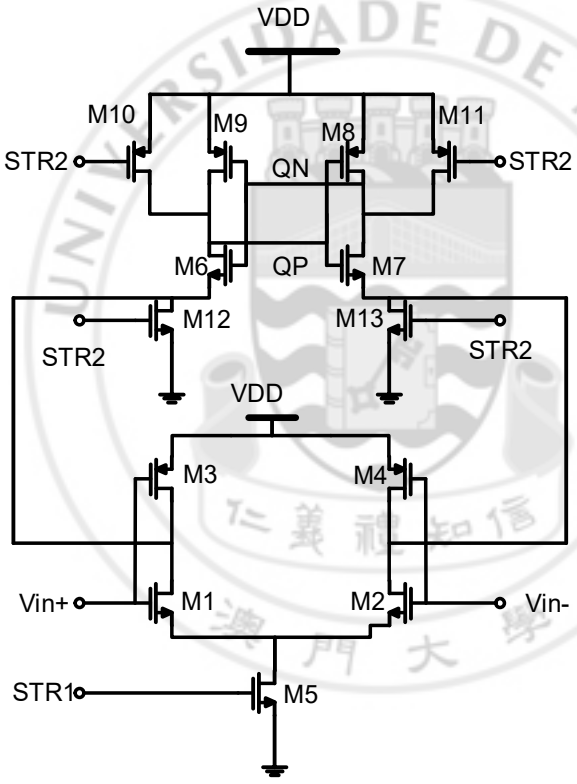

Figure 2.3.9 Circuit schematic of Double tail Low-Noise Dynamic Comparator

The proposed comparator shown in Figure 2.3.9 utilizes different clock signals for the first and second stages which can extend the time in saturation of the input transistors, and improve the speed sensitivity over the input voltage difference and noise performance. For this topology, different clock signals are applied into input stage and regeneration stage in order to expand the amplification time of the input

transistors, and the speed sensitivity over the input voltage difference and noise performance are improved.

The schematic of the proposed comparator is shown in Figure 2.15 and its operation details can be described as follows: during reset phase (STR1=0 and STR2=0) to ground, the intermediate nodes (ti+, ti-) and output nodes (QN, QP) are charged to VDD through M3, M4 and M10, M11 which are turned on by the inputs at around common-mode voltage ; at phase 1 during comparison (STR1=1 and STR2=0), M5 is turned on and a current path from supply to ground through the dynamic inverter (M1~M4) is established. Furthermore, the intermediate nodes (ti+ and ti-) are discharged with a time difference (Δt) depending on the comparator's inputs and the skew rate of the dynamic inverters. During this period, M10 and M11 are still on and they provide other current paths to the first stage through M6 and M7, keeping the input transistor pair (M1, M2) saturated. After the phase 1 of the comparison, STR2 moves to VDD and the back-to-back dynamic inverters (M6~9, M12, M13), in the second stage, regenerate the current difference from the first stage to a logic level VDD or ground at QP and QN.

The outputs of the first stage do not connect to any gate terminal of the second stage transistors. Instead, they connect to the source terminal of M6 and M7, respectively, which provides an extra current branch during phase 1 of the comparison and expands the saturation period of the input pair (M1 and M2). It is easier to identify the improved extension region comparing the small signal parameters of the proposed and former work. When $g_{m1} < g_{ds1}$, the input transistor M1 operates in saturation and it can be observed that the input transistors pair of the proposed comparator stay longer in saturation region than in the comparing one. In large signal behavior, the effect of extending the time in saturation in the proposed architecture implies a larger Δt. [2.8]

The double tail low-noise dynamic comparator achieves a good noise performance. This relies on a great $g_m t/C$ gain. Different from other prototype, there are two pairs of input transistors which are formed by M1 to M4 in this structure contributed the transconductances in comparator. Which can directly improve g_m.

Moreover, an extra pair of current paths is provided through transistors M6 and M7 since the outputs of the inputs sensing stage are changed to connect to the source terminals of the latch stage, the current paths extend the saturation time t of the input transistors M1 and M2. Based on the above two improvements, the overall $g_m t/C$ gain is improved. Also, inputs sensing and latch operate at the same time because they share the current paths and control clock, the time given for comparator is restricted and then the capacity to suppress noise will not be good enough with finite gain. Usually, we have to make a trade-off between speed and resolution. But in the project the resolution is only 8 bits, not such high, so this kind of comparator is suitable for target specification.

2.3.5 DAC Reference Error & Settling Error

The SAR ADC relies on the CDAC to perform the binary-search feedback and switch control. The capacitors in most significant bits (MSBs) are charged or discharged according to the switching nature, it causes large current-induced reference ripples degrading the conversion accuracy. The SAR ADC has a stringent requirement for the precision of the reference voltages. For low-speed SAR ADC the reference error due to switching transient is not problematic, as the SAR loop provides sufficient settling time for the DAC and references. However, this problem is critical in moderate and high speed design, as the time spared for the reference recovery is limited. The reference errors become more significant in ADCs using the TI scheme such as TI-SAR, where the multi-channels share the same reference source and operate simultaneously. The conversion in each channel interacts via the reference source, finally leading to signal-dependent errors that are difficult to be calibrated. [2.8]

The operation of the SAR ADC need the comparison between the input signal and the reference voltage. The different reference voltages are generated by the different switching processes of the DAC array. Because the speed of ADC is very fast, so, the reference voltage may not settle before the comparison is made. That

means, the input signal is not comparing with the correct reference voltage. So the output will not be right anymore. DAC capacitor unsettle is one of the causes of this reference error. It is realized by the equivalent RC network constructed by the switch and the capacitor in the DAC array. Figure 2.3.10 shows the equivalent RC model when the MSB capacitor is charged by the reference voltage. The RC time constant must be small enough to charge the capacitor to V_{DD}. If the time is not enough, the reference voltage will not fully settle down.

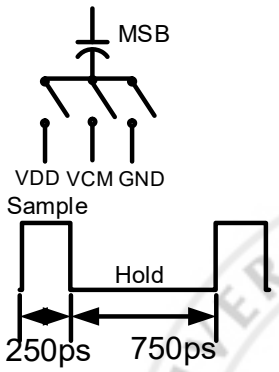

Figure 2.3.10 Equivalent RC model

And

$$\tau = R_{on}C_s$$

R_{on} is depend on the on-resistance of the switch Therefore, there need to pay more attention should be paid for the size of the switch, since the on-resistance of the switch depends on the size of the MOSFET.

Another cause of the reference error is the supply variation due to the inductive bonding generate switching noise. The current transient draws power from the supply voltage, it is necessary for the supply to recover to its original level. Although the RC time constant is small enough, the reference voltage will also trace the supply voltage. Therefore, if the supply voltage is varying, the reference level is also varying. If the comparison is made before the supply recovers, the reference variation will occur, thus causing conversion error.

Both of these reasons will cause the same effect as the reference level is incorrect. Figure 2.3.11 shows a 3-bit V_{cm}-based switching DAC array with a sampling network and a comparator. V_{cm}-based switching is applied in this example. For the sampling phase, all the bottom-plates of the capacitors are connected to V_{cm} while the top-plates

of all the capacitors are connected to the input signal. During the hold phase, firstly, compare the input signals, if the input signal of input_p is smaller than that of input_n, the MSB capacitor of input_p switches to V_{REF} (as V_{DD}) and the MSB capacitor of input_n switches to V_{GND} (as GND) at the same time. Then can get a relative high potential at input_p and relative low potential at input_n, and then do comparison again. Now if there is a DAC settling error, the bottom-plate of the MSB capacitor of p-side cannot fully settle to V_{REF} before the next comparison begin. Assume that the level is V_{REF}-ΔV_1, the top-plate voltage of input_p is not high enough as expected because of a smaller V_{REF}. Under this condition, if the settle time is too small or the time need to settle is too large, it is possible to cause a conversion error. This condition mostly possible happened in the conversion of MSB. If have enough time to let this procedure goes on, the DAC settling error of the MSB capacitor will finally settle to its expected level. Thus, for the second comparison, the bottom-plate of the MSB capacitor is now V_{REF}. However, the DAC settling now occurs at the MSB-1 capacitor. Note that the error voltage is not the same as the MSB case. As stated above, it is related to the power draws by the current transient. Therefore, the error voltage in fact is code-dependent.

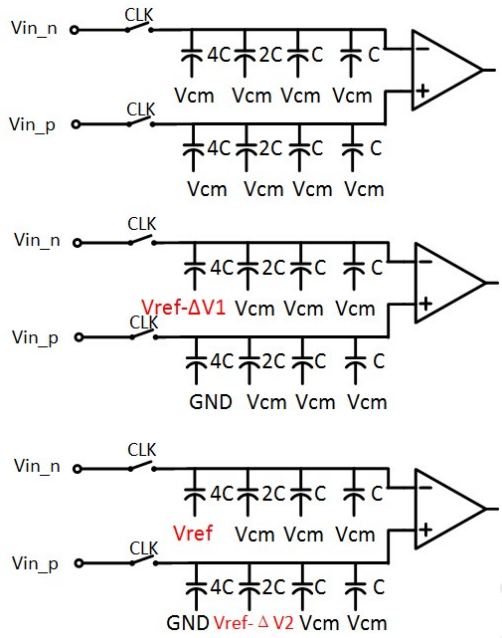

Figure 2.3.11 A 3-bit DAC array showing the phenomenon of the DAC settling error

2.3.6 Solution: Redundancy techniques

Redundancy technique is proposed to solve the settling error and reference error. Redundancy technique is added extra residue LSBs to the DAC array. In order to reduce the error bit.

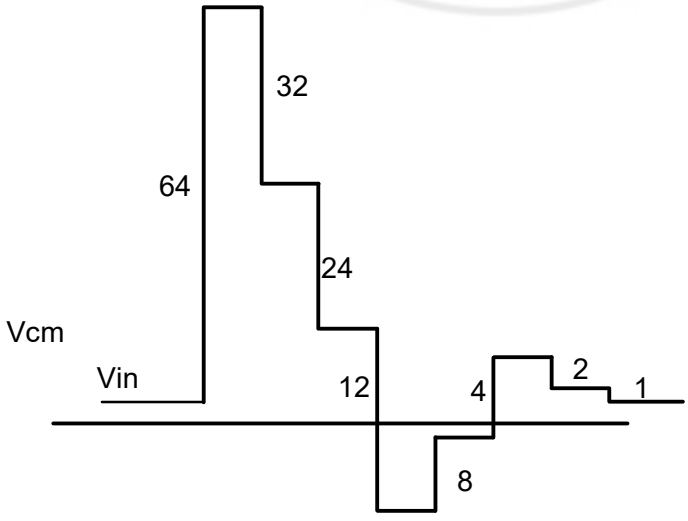

Figure 2.3.12With redundancy operation insight

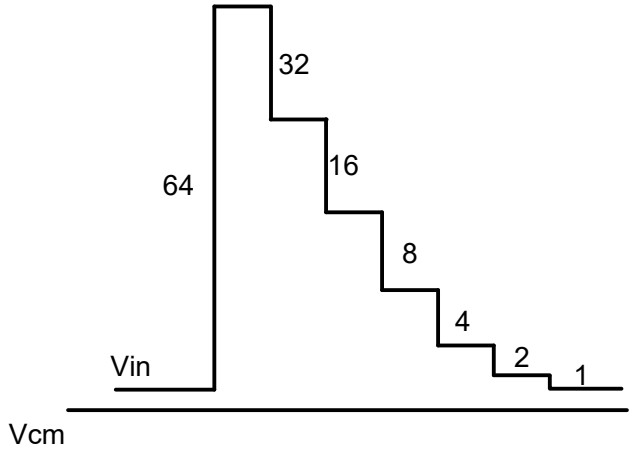

Figure 2.3.13 Without redundancy operation insight

redundancy in this design. The detailed circuit implementations will be discussed in **Chapter 4**.

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Chapter 3 Hierarchical Time-Interleaved Sampling and two-bit per cycle SAR logic

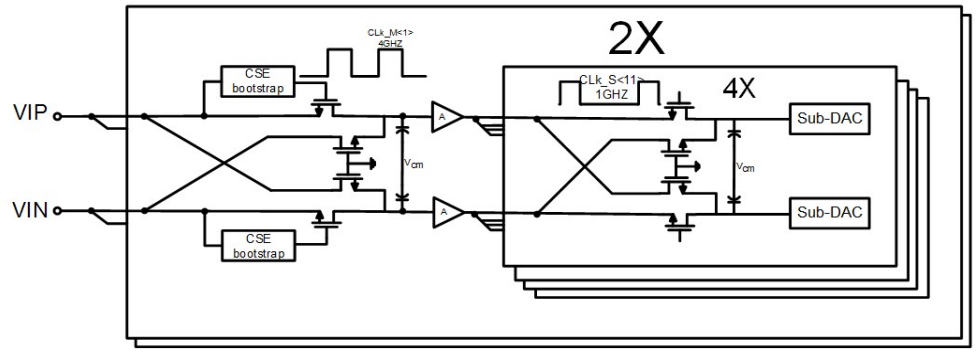
For the [3.1][3.2], the 2nd stage single channel speed is about 1 GHz which is same with the 2nd stage single channel speed proposed in this project. The problem generate in [3.1][3.2] S/H stage is solved by advanced process SOI, which can control the value of Vth that can get a high speed but low resistance, the proposed Hierarchical IT sampling front-end can be implanted in conventional process.

3.1 Introduction of Time-Interleaved

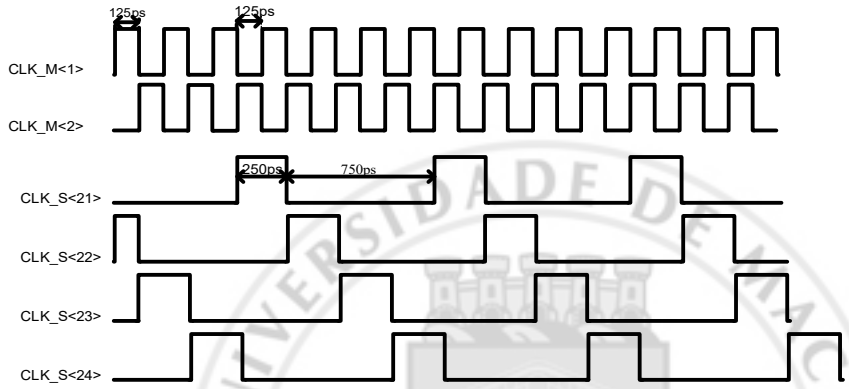
3.1.1 Hierarchical Time-Interleaved Sampling front-end

Time-interleaved sampling is instead sampling the whole signal of sampling the signal with different clock in series with different phases. In this way, the demand speed of each clock reduced, a high speed signal can be sampled by several low speed sampling clock. But due to the jitter problem, the relationship of each sampling clock need to be set very carefully. In this chapter, a 2*4 hierarchical time-interleaved sampling front-end is proposed. Hierarchical time-interleaved sampling front-end can reduce the influence of jitter problem compare with conventional time-interleaved sampling front-end. In this way, the demand of clock can be loosed, for an 8-bit ADC in this project. There only two critical clocks need to be strict design. Rest 8 clocks are not need to such a high level design. This is more convenient for design. In Hierarchical sampling, there are two main stream structures: Buffer structure and charge sharing structure. Next part will introduce them one by one.

3.1.2 The Buffer structure Scheme



(a)



(b)

Figure 3.1.1 (a) Buffer structure scheme front-end architecture (b) Clock diagram

Figure 3.1.1 (a) shows the block diagram of the 2×4 hierarchical time-interleaved multi-bit SAR ADC, in which two interleaved channels comprise the first level of T/H hierarchy. And the interleaving factor for first stage is 2. And behind each channel of first T/H stage, a source follower buffer is connected towards top plate of sampling capacitor, driving four interleaved channels in second level of hierarchy with T/H circuit and multi-bit sub-ADCs. The sub-ADCs are 2-bit per cycle SAR ADC with capacitive DAC array. Interleaving factor in 1st stage T/H is 2, so 1st stage T/H works on the sampling rate of $f_{S\_M}=F_S/2$ = 4 GHz, and only 2 phases are required. So, the clock signals for 1st stage T/H, marked as CLK_M<1> and CLK_M<2> are both 4GHz with 50% duty cycle, and their phase are inversed. The 2nd level of hierarchy has interleaving factor of 4 referred to 1st stage. So clock frequency of 2nd stages is $f_{S\_S}=f_{S\_M}/4$ = 1GHz. The 2nd stages of T/H samples DC level hold by 1st stages, so

sampling time for 2nd stage is equal to hold time of 1st stage, and hold it in the reset time of its cycle as shown in Fig.4.1.2 (b) timing diagram.

a) Master T/H Stage

After time interleaving, for each single signal path in sampling front-end, sampling is done with a relative slow clock and fast signal. This situation leads to an issue that input signal is rapidly changing while T/H module is in hold mode. And the parasitic capacitance of sampling switch provides a sufficiently small impedance compared to the MOSFET channel resistance in off mode, which provides a low impedance signal path for high frequency signals and make signal feed through it to sampling capacitor. This signal feed-through brings undesired charges to sampling capacitor in hold mode and distorts sampling result. To avoid this issue, cross-coupled NMOS switches in the same size of sampling NMOS switches, with gates connect to GND are inserted as shown in Fig.4.1.2 (a). Cross-coupled NMOS switches and sampling NMOS switches are in the same biases while in hold mode, thus an extra signal feed-through with the same amplitude but inverse polarity is introduced to cancel out signal feed-through.

b) Slave T/H stage

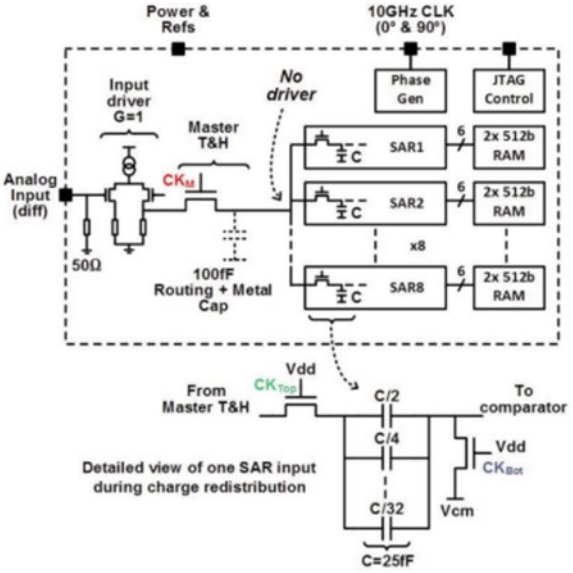
The design procedure of slave T/H stage is similar to master T/H stage with extra concerns on sampling capacitance. Since desired sub-ADCs architecture is 2b/cycle SAR ADC to enhance conversion speed, two capacitive DAC arrays are required. So the equivalent sampling capacitance on 2nd slave T/H stage is the sum of these two capacitor array. To grantee accurate steeling in SA switching operations, small capacitance on each array is preferred. It is highly flavored. Also, the slave T/H modules are driven by buffers, they will affect gain and bandwidth of buffers. Since bandwidth of a source follower which is used as buffer in this hierarchical sampling front-end is g_m/Cs, where Cs is the equivalent capacitance of the capacitive DAC arrays in sub ADCs, a small Cs is preferred to achieve a high bandwidth of buffers. Both requirements lead to a small Cs, so the capacitance of capacitor arrays Cs is set to be just satisfy the requirement of thermal noise.

3.1.3 The Charge Sharing Scheme

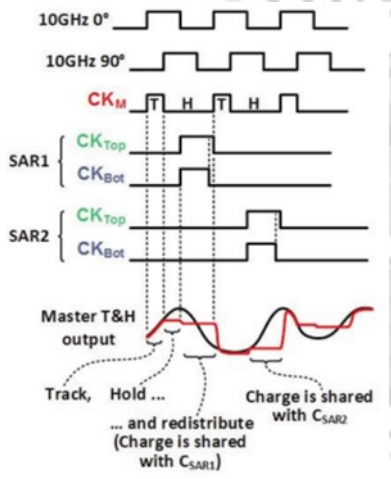
The charge sharing scheme in [3.2] provides a low-power hierarchical sampling solution, benefits from the absence of buffer between different sampling stages as illustrated in Figure3.1.2 from [3.2]. In this architecture, second stage T/H circuit sample at the hold phase of first stage T/H circuit by sharing charges from sampling capacitor of 1st stage. Signal will attenuated in this charge sharing process and the attenuation penalty is

$$\frac{C_{S\_M}}{C_{S\_M} + C_{S\_S}}$$

where C_{S_M} is sampling capacitance of 1st stage T/H circuit and C_{S_S} is sampling capacitance 2nd stage. The signal attenuation leads to a fact that this scheme suffers from the increase of sampling frequency and resolution. Higher resolution requires lower thermal noise floor, which requires a larger sampling capacitance in second stage, and thus a stricter bandwidth requirement for sampling RC network. And to maintain a sufficiently low signal attenuation caused by the charge sharing, the capacitance of second stage sampling should be sufficient small compared to first stage sampling capacitance, otherwise, the attenuation of signal power will cause SNDR drop of the whole ADC. The challenge is that the first stage works on the highest frequency of the whole sampling front-end, but, it requires the largest capacitor in the two stage according to this architecture. Figure 3.1.2 shown the charge sharing scheme in [3.2]



(a)



(b)

Figure 3.1.2 (a) Charge sharing scheme front-end architecture [3.2] (b) Clock diagram [3.2]

3.1.4 Comparison between Two Structures

Buffer structure used in [3.1] and [3.2] could be implemented with similar sized capacitors in first and second stage. The advantage of this kind of structure is sampling capacitor can be relative smaller compare to second type. A smaller sampling capacitor means the standard of sampling switch design can be more relaxed. Because the buffer ability on drive of the back is powerful. But under 28nn process it is very difficult to design a buffer which can guarantee the linearity and gain at the

same time, it needs consume extra power. Another structure is charge sharing structure. This structure doesn't have buffer, second stage sampling capacitor will directly sharing electrons from first stage sampling capacitor. In this way, linearity can be guaranteed. The gain can be controlled by adjusted the ratio of first stage sampling capacitor and second stage sampling capacitor. Signal will attenuated in this charge sharing process and the attenuation penalty is $\frac{C_{S\_M}}{C_{S\_M}+C_{S\_S}}$, where C_{S_M} is sampling capacitance of first stage T/H circuit and C_{S_S} is sampling capacitance second stage. The signal attenuation leads to a fact that this scheme suffers from the increase of sampling frequency and resolution. In this structure, the size of first stage capacitor is relative large, the capacitance of second stage sampling should be sufficient small compared to first stage sampling capacitance, otherwise, the attenuation of signal power will cause SNDR drop of the whole ADC. But under this project sampling frequency, the effect is invisible. So it can ensure have a same gain with buffer structure and have a very good linearity at the same time. This is the reason why choose this structure. For this structure, first stage is very critical to the time. But for the second stage it is not that serious for the time, for an eight branches interleaving it only need 2 critical clock in the second stage. This is because of the second stage actually is sampling a DC voltage potential so the second stage is not such critical to the time. This is the reason we chose this structure. In the previous references [3.1] [3.2] their second stage clocks need to have very good match and critical time shift. And in these cases, based on SOI process not based on standard CMOS process. In this way, they can through adjust the V_{th} to a relative low level to decrease on resistance, sampling capacitor can track the signal perfectly. The reason is the Supply-V_{th} is positive correlation with sampling linearity. The supply is constant, so decrease the value of V_{th} can improve the linearity of sampling. In this project we want to find a solution can implement in the standard process. In the previous references, due to the benefit of process, they didn't add bootstrap circuit to sampling circuit. So in this project, there have bootstrap circuit to the first stage to ensure a high linearity.

V_{GS}=supply-signal，

V_{GS}-V_{th}= supply-signal-V_{th}

The value of V_{GS}-V_{th} is negative correlation with Ron. The fluctuation range of V_{GS} is also the fluctuation range of signal. This value divided by overdrive can be approximated us the fluctuation range of Ron. The larger fluctuation range the worse linearity. Bootstrapped circuit make V_{GS} is a constant value to eliminate several of overdrive to improve the linearity. Another benefit of bootstrapped circuit is fixed the value of parasitic capacitance C_{gs} and C_{gd}, clock feed-through is static state not dynamic. In this project, there have another switch after first stage sampling switch this is to eliminate the signal clock feed-through. The signal will through the sampling switch C_{ds} feed-through to sampling capacitor during the hold stage. So after the sampling switch there has another switch has the same size but source terminal is inversed with sampling switch. To provide an extra C_{ds} but have inverse phase to complement the signal clock feed-through. At the hold stage the gate terminal of this switch will connect to the ground. The second stage is sampling electrons from first stage sampling capacitor directly. Because of it is sampling from a DC voltage potential, only requirement is to finish the sampling process not out the time window, so the clock is relative relax in the second stage.

3.1.5 Channel-Selection-Embedded Bootstrap Circuit

CES bootstrap proposed in [3.3] which minimizes the master clock path to the bootstrap terminal by simply performing the channel selection in the bootstrap itself. The series connection between the master and slave switches avoids the time skews among the sub-channel's sampling. The disadvantage is the reduced bandwidth which can be traded by using larger sized sampling switches. The Figure 3.1.3 shows the sampling instances in the main channel is defined by a common-master clock, which is applied directly to the transistor M2. The transistor M1 is used to enable the channel according to the clock signal Φ_s. The solution avoids the additional devices such as MUX or AND gate implemented in series with the master clock signal, which minimizes the clock jitter injected in the main clock path to the bootstrap terminal.

The 1st (2nd) channel starts to track the input signal, when Φ_1 Φ_2 is high. Either of the channels stop tracking, while M1 and M2 are both turned on. The sampling instance is determined by the rising edge of Φ_m that pulls down the gate voltage of the sampling switch from $V_{in}+V_{dd}$ to ground. The transistor M3 is assisted to avoid the floating of $V_{B1(B2)}$, which is not necessary if the floating duration is short. The master clock is generated via an inverter chain generator. It is routed separately to the gate terminal of M2 in the main S/Hs, if which the distances are optimized and symmetrical routing is implemented to guarantee a good matching between two master clock paths.

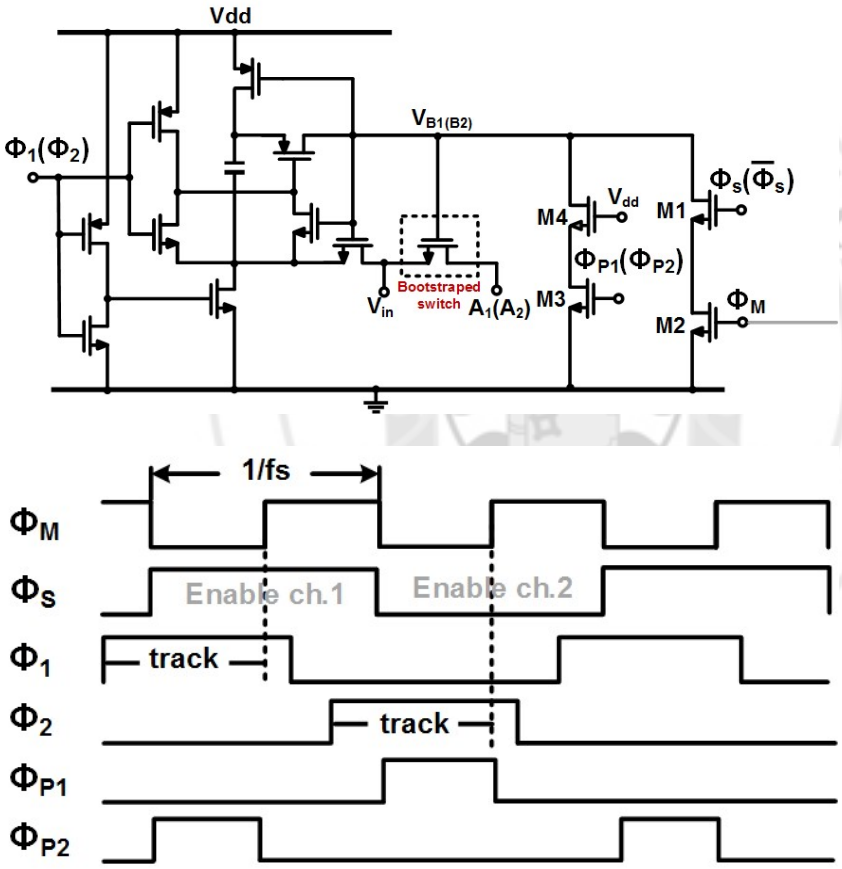


Figure 3.1.3Proposed channel-selection-embedded bootstrap circuit and its control timing diagram

3.2 Two-bit per cycle SAR logic

3.2.1 Introduction

The technology of integrated circuit has been improved fast. The chip has been greatly enhanced from 65 nm to 28nm. For 65 nm technology, the technology node features the maximum supply voltage is only 1 V for the standard MOS transistors, and the supply voltage is decreased to be 0.7 V for the 45nm. However, as the device threshold voltages do not scale proportionally with decreasing supply voltage, the available voltage swing decreases which effectively disallows the use of stacked MOS circuit configurations [3.4]. The device transition frequency f_T as well as the bandwidth of analog circuits, are increases with each new technology node. Unfortunately, decreasing the feature size also decreases the Early voltage VA and hence the device output resistance ro. Decreasing channel resistivity leads to decreasing intrinsic DC gain ($A_0 = g_m r_o$), thus reducing the inherent circuit accuracy [3.5]-[3.6].

Although the reduced analog performance, especially in terms of gain, may be reflected in increased power consumption for a desired ADC accuracy, the circuit complexity increases to compensate for intrinsic technology shortcomings [3.7].

3.2.2 Architecture

For high-speed ADCs, when the required sampling frequency approaches the maximum value allowed for a given technology, the number of clock cycles required for achieving a conversion becomes a severe limitation for the sampling, the input voltage is hold on the top of the capacitor array. Then, the first two capacitors of these four cap arrays will be charged or discharged, and the first comparison result will be determined. Based on the result, the corresponding switch will have next movement. For each comparison, the comparator will give 3 digits, therefore an encoder is

required to change the 3 digits into 2 digits and pass to the register to store. The total process will take M/2 cycles before the last two bits are determined.

3.2.3 Characteristic

For high-speed ADCs, when the required sampling frequency approaches the maximum value allowed for a given technology, the number of clock cycles required for achieving a conversion becomes a severe limitation for the exploitation of the SAR ADC power efficiency and other less power efficient topologies have to be used [3.7]. Generally, based on the theory of parallelism, two solutions are proposed. They are time-interleaved structures and increase of number of bits resolved in each cycle by the SAR topology.

Therefore, the most noticeable characteristic of 2 bit per cycle logic is high speed. However, as the reference standard is set by the subtraction of these capacitor arrays, the unsettling problem may affect more.

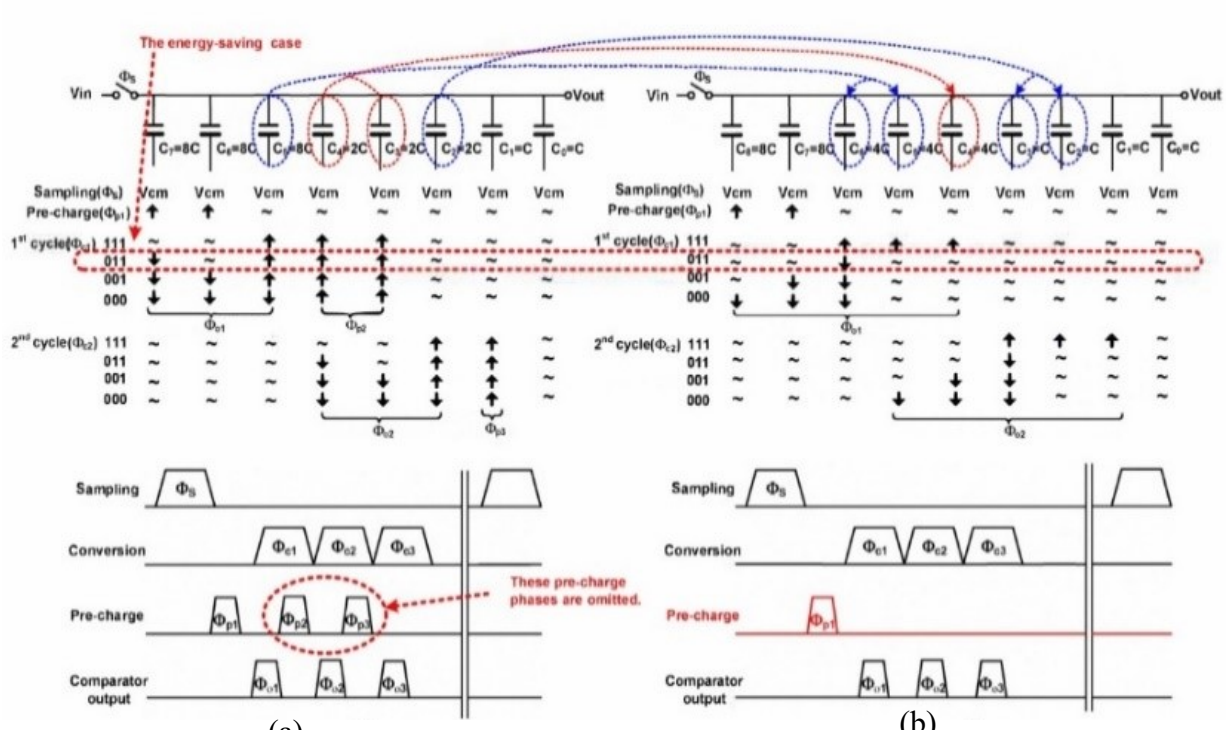
3.2.4 2-Bit Per-cycle SAR Switching

The A/D converter switching controls the movement of capacitors in order to set expected voltage on top of capacitive DAC array and then, deliveries it to comparator. Compared with single bit conversion scheme, multi-bit conversion has a faster speed but extra complexity. A 2-bit SAR ADC with multi-merged switched redundant capacitive DACs is proposed in [3.8].

Figure 3.2.1 (a) Conventional 6-bit Capacitive DAC array [3.8] (b) The 6-bit redundant capacitive DAC array proposed in [3.8]

Figure 3.2.1 shown a switching demonstration from [3.8] comparing conventional capacitive DAC array and merged redundant capacitive DAC array proposed in [3.8]. (a) Conventional 6-bit Capacitive DAC array (b) The 6-bit redundant capacitive DAC array proposed in [3.8]

In the conventional switching sequence, at the start of each conversion cycle, a pre-charge phase is required. Besides, based on the results given by comparator, the control circuit may have charging and discharging at the same time. This large switching transient will cause problem like excessive supply voltage undershoot, potentially exacerbating an overdrive condition of the preamplifier, namely, a wrong decision may happened to the comparator's output. However, the multi-merged switch is free from the trial-and-error search procedure, by using this method, the "up" or "down" transitions of the capacitors can be directly given out after each 2-bit decision. Moreover, this method also avoids 'up' and 'down' movement simultaneously, which grantees a fully settled voltage on top plate of capacitor array. Details of the switching is illustrated in Figure 3.2.1 and Figure 3.2.2 shows the performance comparison between conventional DAC and multi-merged DAC in both (a) settling speed and (b)

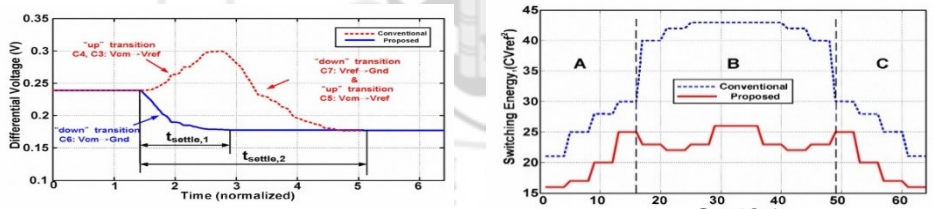


switching energy.

Figure 3.2.2 (a) Settling comparison [3.8] (b) Switching energy comparison [3.8]

In the multi-merged switch method, V_{cm}-based switching [3.9] is utilized enabling high speed and low power SA operation in ADC. The V_{cm}-based switching method guarantees a mismatch free MSB determination and saves capacitor area at the same time with the absence of MSB capacitor. Besides, in each bit cycle, the charge-recovery makes switching energy lower than other methods, such as charge-recycling and set-and-down.

Moreover, the reference-free implementation and the passive multiplication by 2 avoid the use of the power-hungry resistive ladder/reference buffer without imposing a rail-to-rail input. The result is a fast RC settling and low power dissipation during SA conversion in the capacitive DAC array. As in the method of V_{cm} based switching, the common mode voltage does not change, therefore it ensures the stability of the

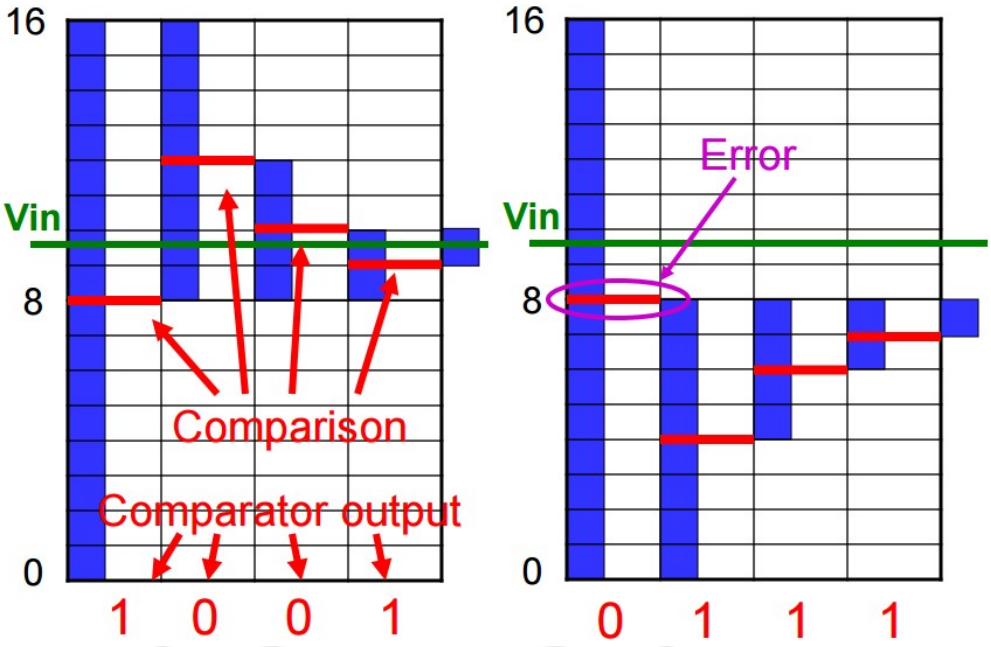


voltage in the reset part and make the debugging easier. Also, it also reduces the requirements in design of comparator, which means the significance of non-linear problem is alleviated.

Figure.3.4 Performance comparison for (a) settling speed (b) switching energy between conventional capacitive DAC array and multi-merged-switched capacitive DAC array proposed in [3.8].

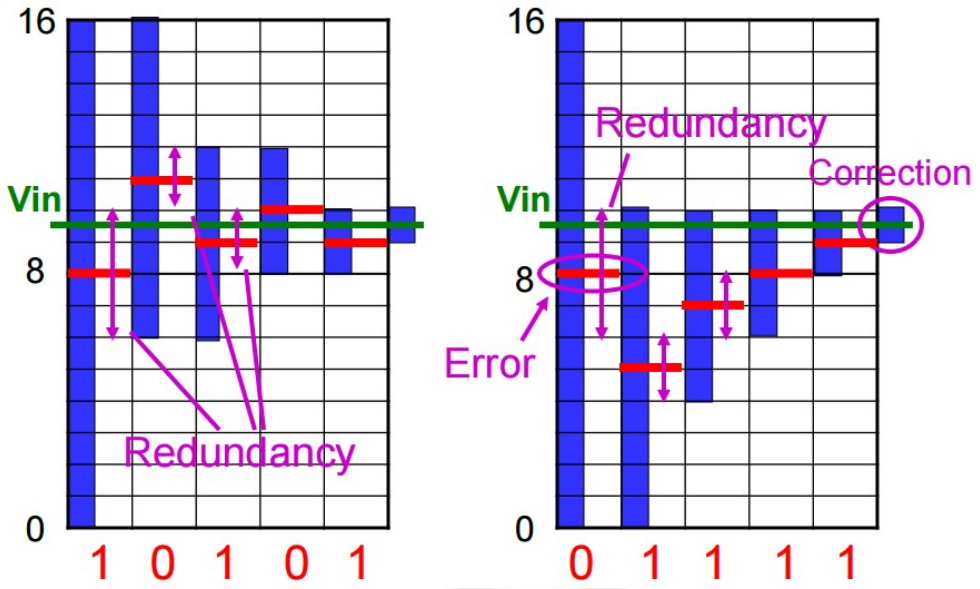
3.2.5 Redundancy

Redundancy is a very useful way to improve the accuracy of ADC. Add extra residue in DAC array to compensate the unsettling condition in the conversation process to reduce the error. Take a four bit SAR ADC as an example. Figure3.2.1 shows the binary search algorithm, and the problem of binary search algorithm with the settling error occurrence. Figure 3.2.2 shows the search algorithm with redundancy under the same condition. The comparison of Figure 3.2.1 and Figure 3.2.2 shows that the redundant SA operation could tolerate a certain level of error.



(a) (b)

Figure 3.2.1 (a) Binary search algorithm without error [3.9] (b) Binary search algorithm with error [3.9]



(c)

(d)

Figure 3.2.2 (c) Search algorithm with redundancy and no error [3.9]

(d) Search algorithm with redundancy and error [3.9]

For the binary search algorithm, 4 bits needs 4 steps to finish the comparison.

Dout= $2^3+2^2\cdot d1+2\cdot d2+1\cdot d3+0.5\cdot d4-0.5$,

where radix is 2 $d_k = +1$ or -1

For Conventional non-binary search algorithm, 4 bits needs 5 steps to finish the comparison.

Dout= $2^3+\beta^3\cdot d1+\beta^2\cdot d2+\beta\cdot d3+1\cdot d4+0.5\cdot d5-0.5$

Where radix $\beta=2^{\frac{3}{4}}$ $d_k = +1$ or -1

The principle of error correction is shown as below:

For binary search algorithm

Comparator output: 1001

$D_{out} = 8+4-2-1+0.5-0.5=9$

For Non-binary search algorithm

Comparator output: 10101

D_{out} = 8+3-2+1-1+0.5-0.5=9

Comparator output: 01111 (error)

D_{out} = 8-3+2+1+1+0.5-0.5 =9

It can be concluded that non-binary search algorithm has multiple codes that leads to same result, namely a certain level of error can be tolerated.

Compared with the conventional non-binary search algorithm, another algorithm named as generalized non-binary search algorithm [3.9] is optimized as it has more flexible radix.

For Conventional non-binary search algorithm

$D_{out}= 2^3+\beta^3\cdot d1+\beta^2\cdot d2+\beta\cdot d3+1\cdot d4+0.5\cdot d5-0.5$

Where radix $\beta=2^{\frac{3}{4}}$ d_k = +1 or −1

For generalized non-binary search algorithm [3.9]

$D_{out}= 2^3+\gamma_1\cdot d1+\gamma_2\cdot d2+\gamma_3\cdot d3+\gamma_4\cdot d4+0.5\cdot d5-0.5$

Where radix are not restricted toβd_k = +1 or −1

Design method of generalized non-binary search algorithm [3.9] is shown as below

If the target A/D converter has N-bit, it will needs M-step (M>N)

First of all, the redundancy needed to be determined.

$2^M-2^N=\sum_{I=1}^{M-1} 2^I qi$

q_i represents the redundancy at i-th step

Secondly, calculate step of reference voltage.

$p_{k+1} = -q_k +2^{M-k-1}-\sum_{I=k+1}^{M-1} 2^{i-k-1} qi$

Algorithm [3.9] is optimized as it has more flexible radix.

For Conventional non-binary search algorithm

$D_{out}= 2^3+\beta^3\cdot d1+\beta^2\cdot d2+\beta\cdot d3+1\cdot d4+0.5\cdot d5-0.5$

Where radix $\beta=2^{\frac{3}{4}}$ d_k = +1 or −1

For generalized non-binary search algorithm [3.9]

$D_{out}= 2^3+\gamma_1 \cdot d1+\gamma_2 \cdot d2+\gamma_3 \cdot d3+\gamma_4 \cdot d4+0.5 \cdot d5-0.5$

Where radix are not restricted to$\beta d_k = +1$ or -1

Design method of generalized non-binary search algorithm [3.9] is shown as below

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q_i represents the redundancy at i-th step

Secondly, calculate step of reference voltage.

$p_{k+1} = -q_k +2^{M-k-1}-\sum_{I=k+1}^{M-1} 2^{i-k-1} qi$

In Figure3.2.3, an example of generalized non-binary search algorithm is given.

But one thing need to remember is that the redundancy will need more time in conversion process. It is a tradeoff need to make between speed and accuracy.

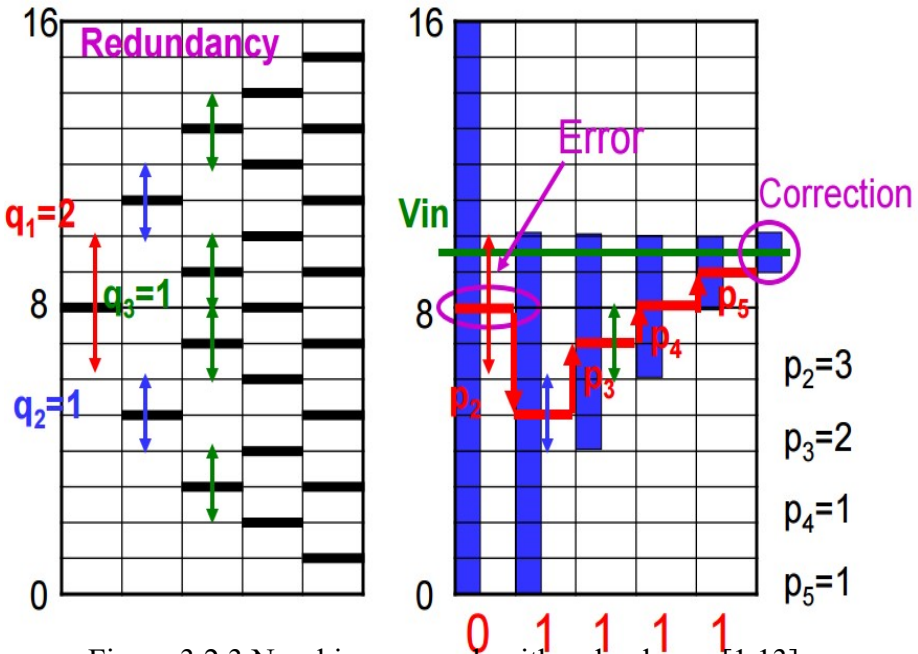

Figure 3.2.3 Non-binary search with redundancy [1.13]

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Chpater4 Circuit Implementation

4.1 Overall ADC Architecture

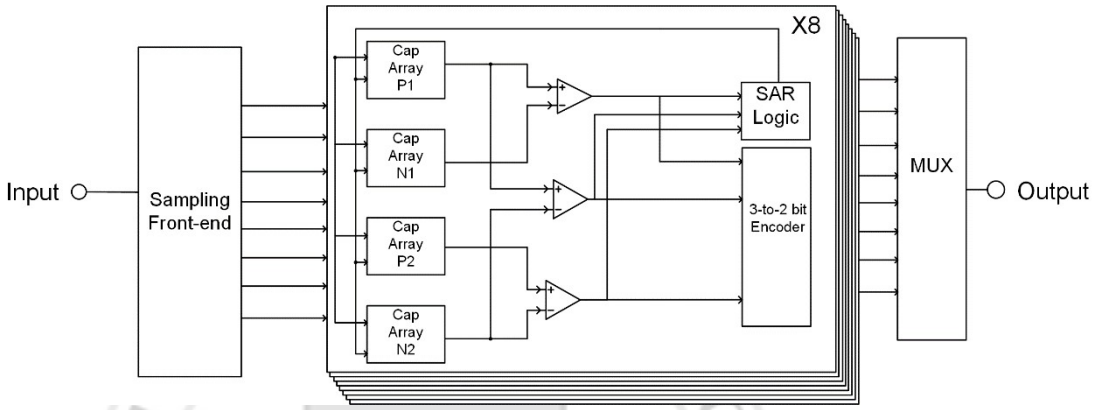

Figure4.1.1 Overall ADC Architecture

The Figure 4.1.1 shown the overall ADC architecture, the input sampled signal will be caught by four capacitor arrays. And then through three comparator to do comparison then the comparison output will be transferred to 3-bit to 2-bit Encoder and SAR logic parallel. The 3-bit to 2-bit Encoder will encode three comparison result to 2-bit output. And then the register will record the output result and give DAC compose output. And finally output eight 2-bit per cycle signals, using MUX to combine them together to get an 8 bit output.

4.2 Proposed Hierarchical Time-Interleaved Sampling front-end

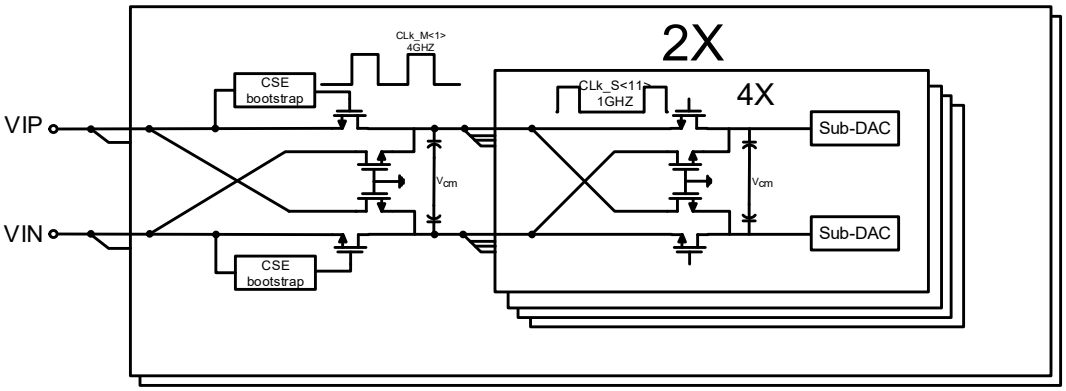

Figure 4.2.1 Hierarchical Time-Interleaved Sampling front-end

Fugure 4.2.1 has shown the architecture of sampling front-end apply in this project. A charge sharing architecture are used in this project. In this project the specification of speed is 8 Hz, the idea is to set a eight branches at ouptut of inter-leaved front-end. So there are two main branches at first stage of hierachical time-onterleaved sampling front-end and each main branches will be septerated into four branches in second stage. The bootstrap circuit is used at the first stage switch. This is because the clock at first stage need to be critical. The bootstarp circuit used in this project can supply the same down edge to different clocks it can reduce the influence of jitter and can make on resisitant be constatn at the same time. For the second stage, it just share charge from first stage directly so the demand of clock is not such critical. And also don't need extra bootstrap circuit. At first the charges are sampled on the first stage sampling capacitors and the second actually is sharing charges from a DC voltage signal. Then the sampling output will transport to DAC array by eight second stage branches.

4.3 Proposed Two-Bit Per Cycle DAC SAR Logic with Redundancy

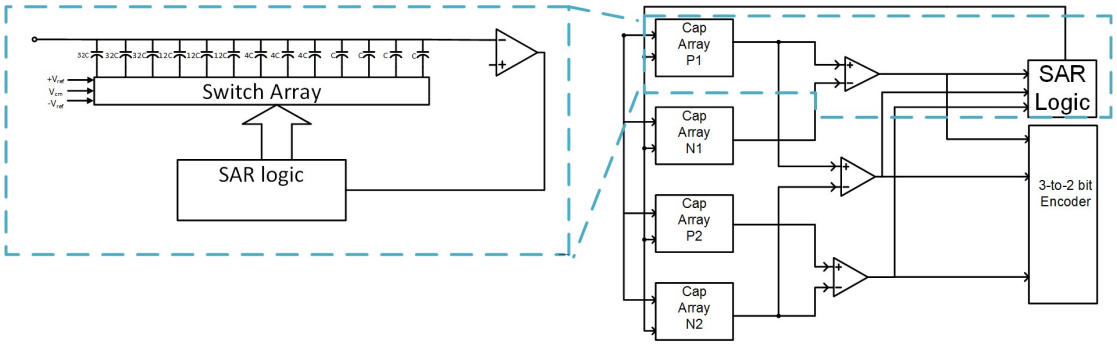

Figure 4.3.1 Two-bit per cycle DAC array

The Figure 4.3.1 Two-Bit per cycle DAC array shown the DAC array used in the project. Each capacitor of the arrays has three swithes. One is connected to V_{ref+} one is connected to V_{cm} and final one is connected V_{ref-} this is due to the actual voltage swing is smaller the input, so the positive and negative reference need to be set. The capacitors are divided in to four groups, each group has three capacitors, the capacitance of each capacitor in one group are the same. The values are 32C, 12C, 4C, C, in this way can tolerate top plate voltage settling error. And there are 20C redundancy added which can tolerate 15.6% error. The redundancy distribution is shown as Figure 4.3.2.

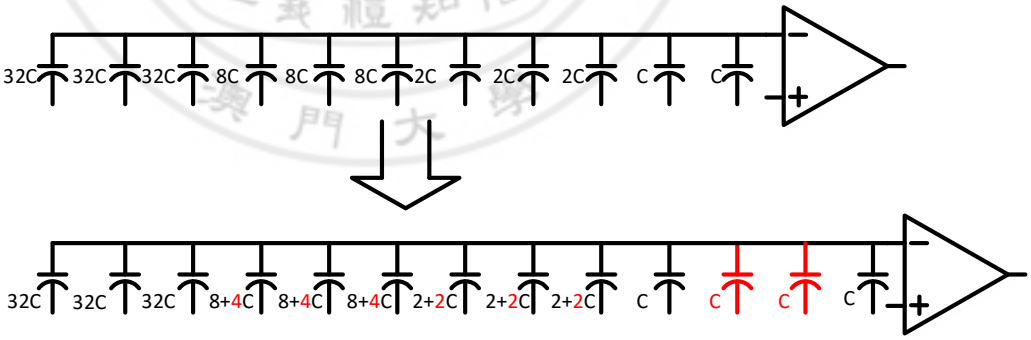

Figure 4.3.2 Redundancy distrubution

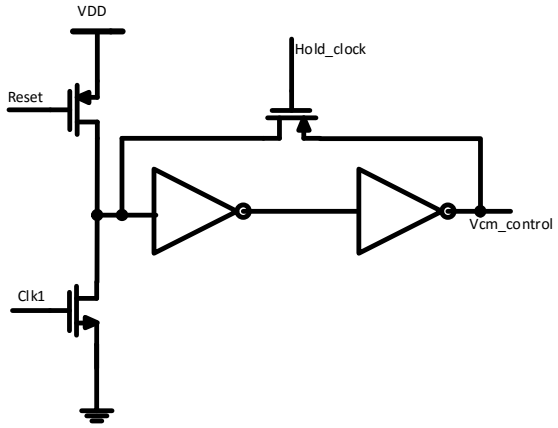

Figure 4.3.3(a) Dynamic control logic(a)

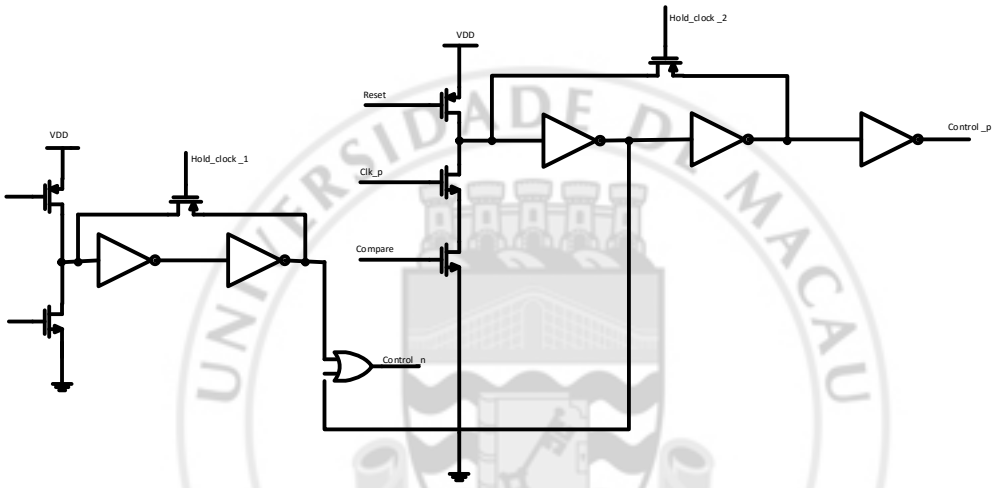

Figure 4.3.4(b) Dynamic control logic(b)

The Figure 4.3.2(a)-(b) are shown the control logic of DAC array. Figure 4.3.3(a) Dynamic control logic(a) is dynamic logic to control Vcm. In the dynamic logic a switch added above to the control logic. This switch is used to maintain the polar of the two terminals of logic circuit are the same. This switch is used to compensate the leak charge from parasitic cap to prove the correctness of output voltage. The dynamic logic using the parasitic capacitor of MOSFET. The hold clock must set low before the before the signal come in. otherwise the control logic can't work normally. The Figure 4.3.3(b) Dynamic control logic(b) is the control logic for capacitor connect to "high"—V_{ref_p} and "low"—V_{ref_n} .The switch array for each capacitor are the same. The full scale of input signal is 0.7 V. But VDD to GND full scale is 1V so there have to set extra "high" and "low."

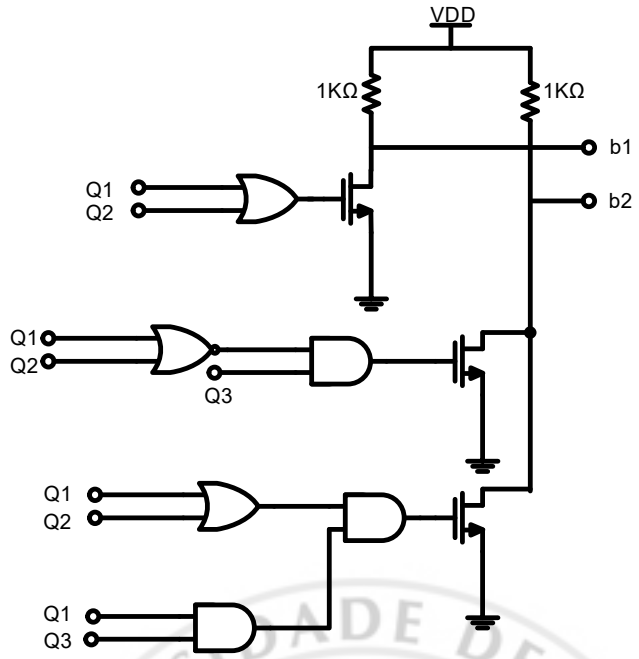

Figure4.3.5 3-to2 bit encoder

The Figure4.3.5 is '3-to-2 bit encoder' used to generate 2 bit output for each cycle. When the comparator gives out the result, there have three comparator, therefore a converter is needed to transform the three digital numbers into corresponding two digitals.

4.4 Double tail Low-Noise Dynamic Comparator Architecture

This comparator not only need to give the positive difference but also the negative difference. There an extra current path through M6 and M7 to expand the amplification time. The M1-M4 formed a high g_m amplifier. But under 28nm the resolution of this comparator only 1 mV. The demand of minimum resolution in this project is about 500 uV. So there need an extra amplifier to enhance the input signal before comparison.

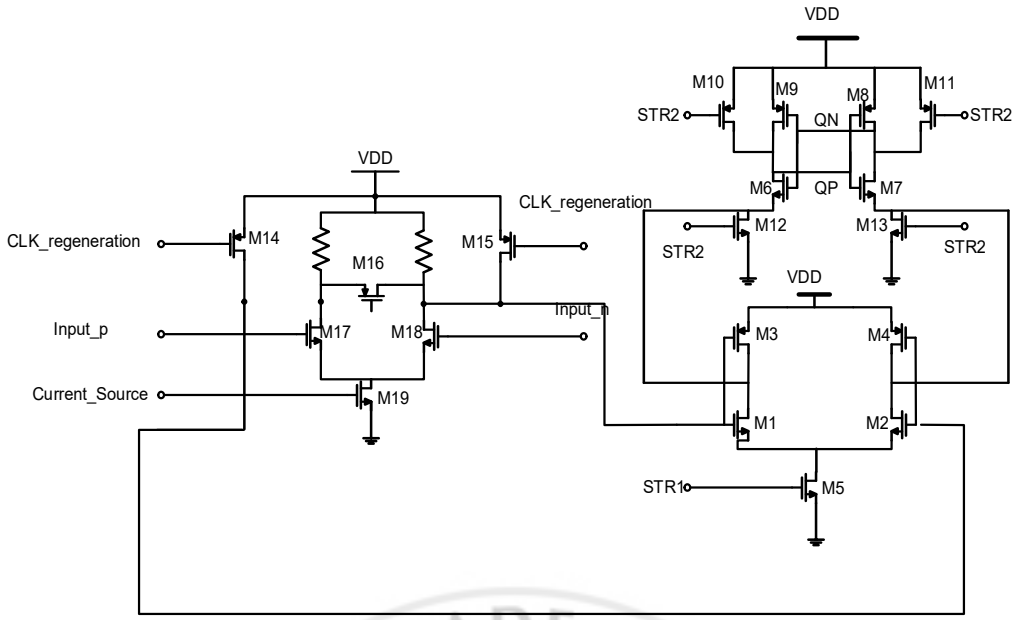

Figure 4.4.1 comparator diagram

4.5 Clock diagram

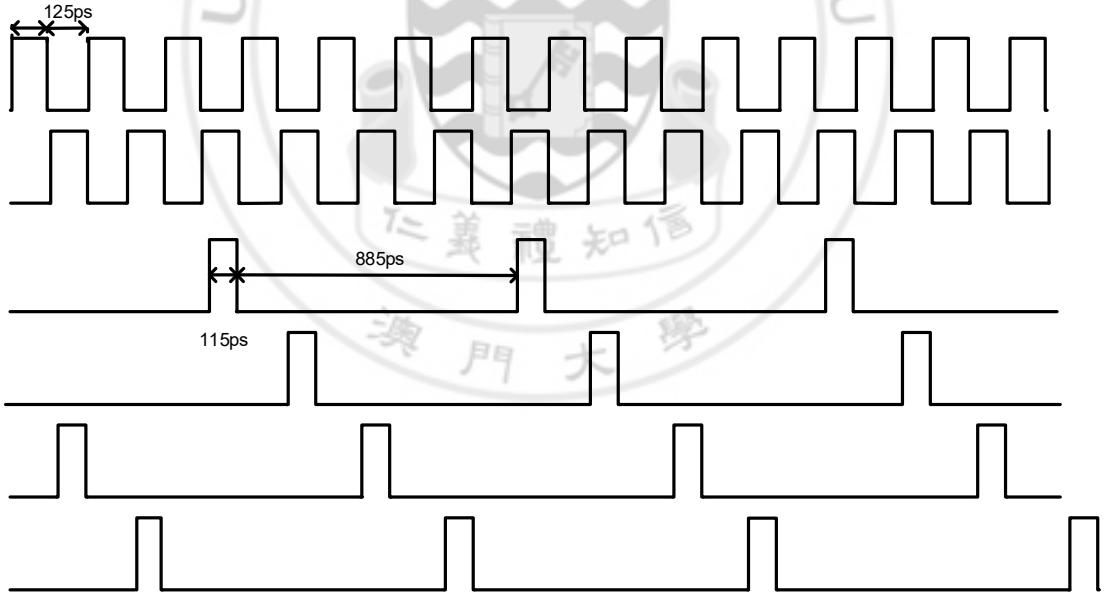

Figure 4.5.1 Clock diagram for Fornt-end

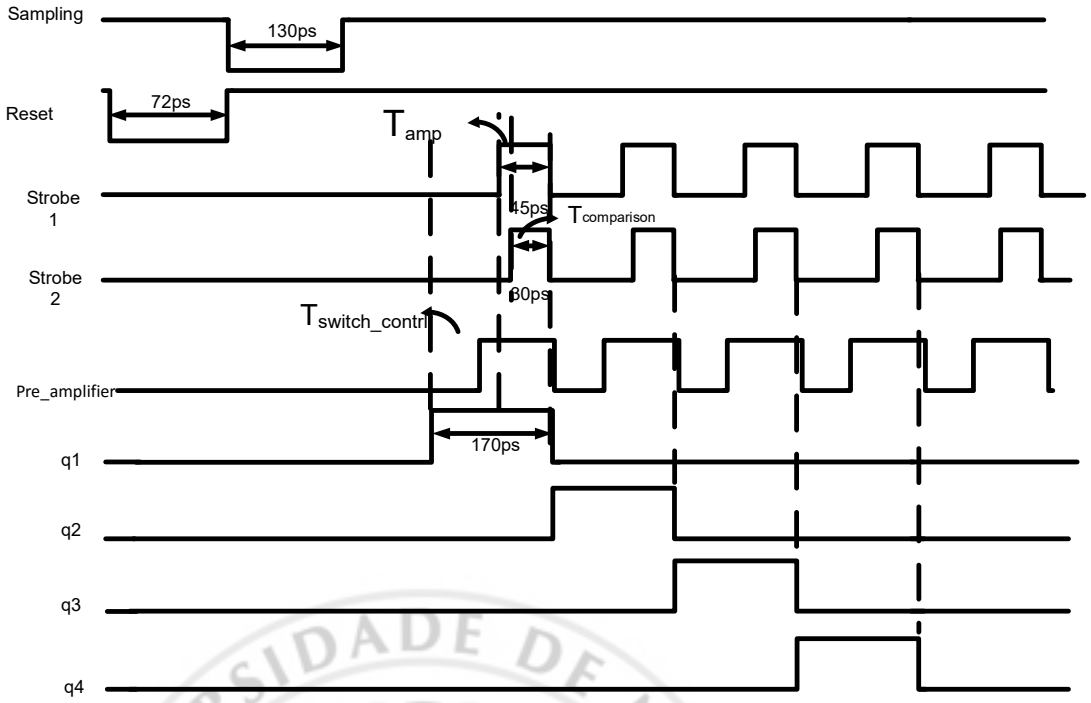

Figure 4.5.2 Total Clock of SAR logic with comparator

Figure 4.5.1and 4.5.2 shown the time loop of the SAR ADC. At the beginning of the comparison we need to reset the comparator first. Then sample the signal, in each SAR logic cycle, there have four arrays: q1, q2, q3, q4. They will action one by one, the time pulse width are the same is 170ps and with the same phase. This is working different interleaved branches connected DAC array. Strobe will act at the end of each q1, q2, q3, q4 pulse. The strobe2 wave is used to do the comparison, and the exceed part of q signals are used to control the switch in the logic circuit. The pre-amplifier need to open before the comparator work and close after the comparison. In order to keep the amplification performance keep constant during comparison process.

Chapter 5 Simulation Result

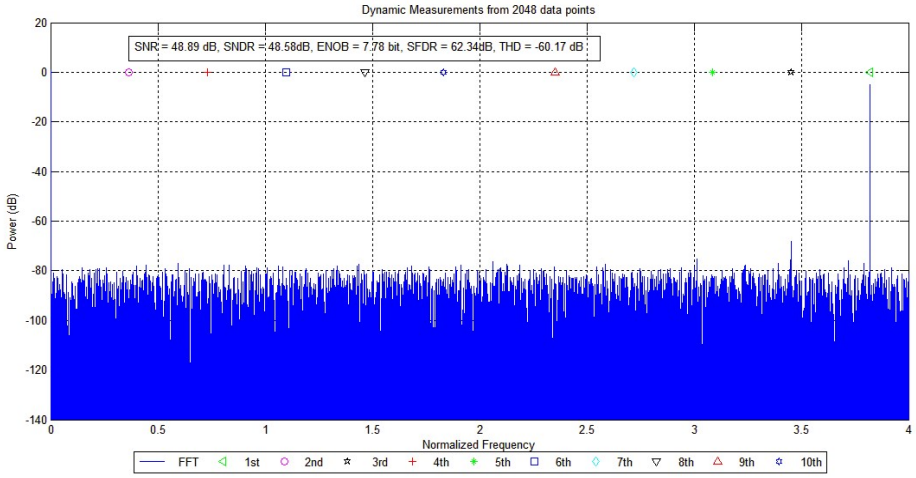

Figure 5.1 FFT analysis without comparator noise

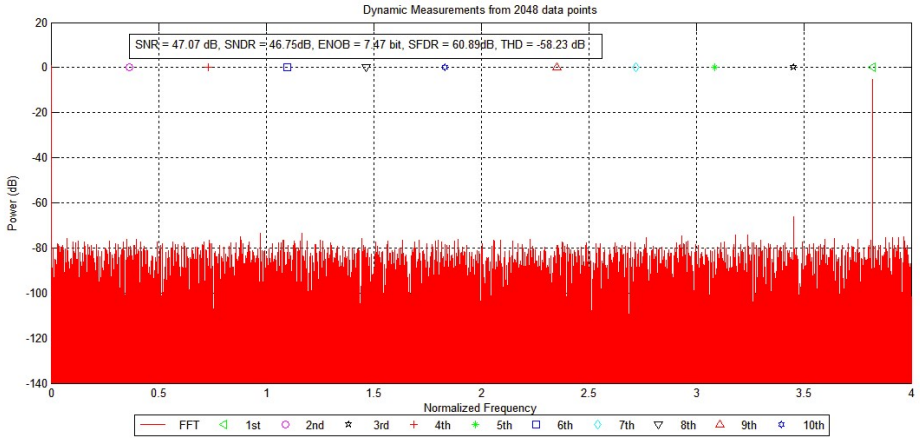

Figure 5.2 FFT analysis with comparator noise

An 8-bit 8-GS/s SAR ADC is designed in 28 nm CMOS using the hierarchical interleaved front-end and two-bit per cycle logic. Time-interleaving front-end and two-bit per cycle logic are proposed to increase the speed of ADC. Dynamic logic is added to further improve the speed of ADC. Redundancy is proposed to compensate the top plate voltage settling error. CSE-bootstrap circuit is adopted to cooperate with hierarchy technique to minimize the timing mismatch and jitter.

Figure 4.6.1 shows simulation result without comparator noise that this approach can achieve SNR=48.89dB, SNDR=48.66dB, SFDR=62.8dB, ENOB=7.78 bits, THD=56dB with input frequency is 3.81 GHz.

Figure 4.6.2 shows simulation result with noise. Under this condition, proposed architecture can achieve SNR=47.07dB, SNDR=46.75dB, SFDR=60.89dB, ENOB=7.47 bits, THD=-58.23dB with input frequency is 3.81 GHz. Furthermore, the power dissipation is 57.54 mW, achieving the FoM of 41.99 fJ/conv.step.

Compare with result with and without noise, the result almost the same. That means the proposed architecture meet expectation designed before. SNDR only 1 dB decrease.

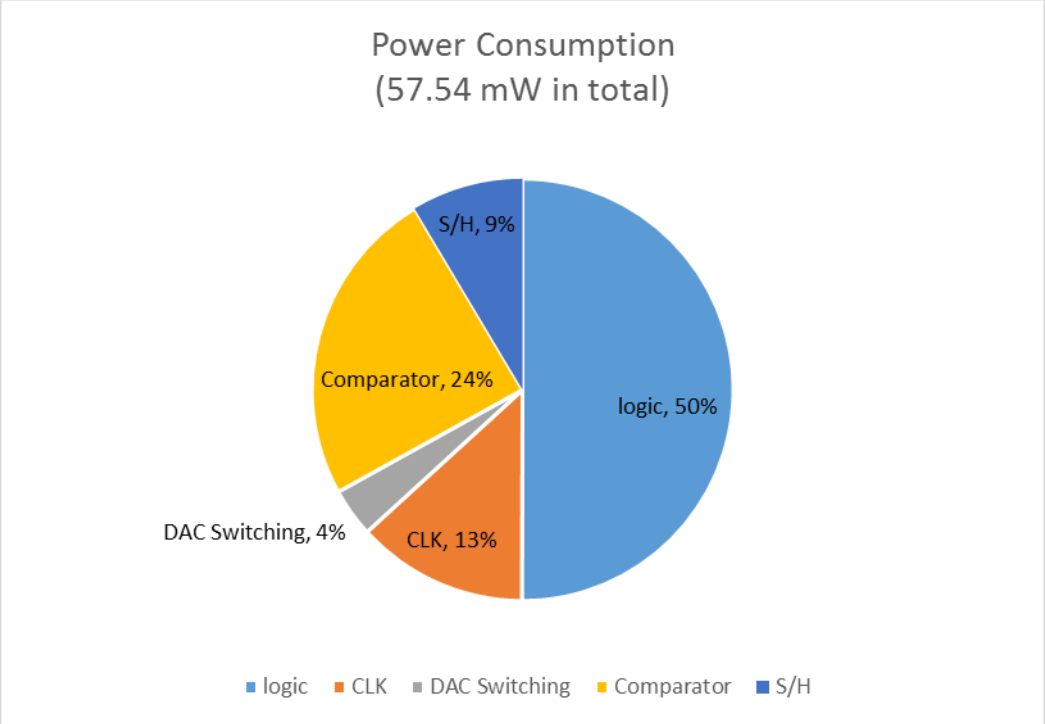

Figure 5.3 Power consumption distribution

	total(8 channel) (mW)
logic	28.81
CLK	7.58
DAC Switching	2.15
Comparator	14.08
S/H	4.93
total	57.54

Figure 5.4 Power consumption

The power consumption figure shows in Figure 5.3 and 5.4. The two-bit per cycle SAR logic part takes 50% of energy. This is due to the characteristic of SAR ADC and there have 8 2nd stage channels. And each channel is connected to 4 DAC arrays and 32 DAC arrays in total. The logic part power consumption is such large.

Chapter 6 Conclusion

Nowadays, the widely apply of electrical devices promote ADC have higher speed and resolution. Under this motivation promoting, this thesis target an 8-bit 8GHz SAR ADC. This high resolution and high speed ADC can be widely used in communication system and broadband satellite domain. In order to achieve such a high demand. Two main techniques are proposed--hierarchical time-interleaved front-end and two-bit per cycle logic combined with digital error correction. Time-interleaved front-end is widely used in high speed ADC, while bringing critical requirements on clock signals at moderate and high resolution. It conventionally need to burn extra power to design critical clocks for time-interleaved front-end. Hierarchical interleaved front-end can reduce the influence of jitter and the demand of clock can be loosed and easier to design. Two different types of time-interleaved front-end were compared to show the advantages and disadvantages.

In the previous study, for hierarchical inter-leaved circuit design, SOI technology was using on chips [1][2]. In this way, threshold voltage can be set as desired value. Then base on this advance, sampling front-end can have a good linearity. In this project, CSE-bootstrap circuit is introduced and it can solve the problem in conventional craft. CSE-bootstrap circuit can keep the r_{on} be a constant and also can supply different phase sampling clock with one master clock. In this project, SAR architecture ADC was selected because of its advantages over other types of Nyquist ADCs. Under target resolution and speed, SAR architecture is the most balance one compare with other architectures such as pipelined ADC or flash ADC. It can generate an n bits output just use n cycles. So the speed is fast. With the help of two bit per cycle logic, the ADC will output two bit in one cycle, further enhanced the speed. In order to reduce bit error, redundancy is added in to DAC array. Redundancy can compensate the error bit problem obviously, although it need an extra cycle. Another very important part of ADC is comparator. In this project, double tail low-noise

dynamic comparator is used with pre-amplifier. This kind of comparator has a good ability to resist noise and has an extra current path to expand amplification time. Pre-amplifier is to make the comparator achieve the need minimum resolution.

Finally, the actual circuit implementation was discussed, the proposed comparator was presented and the corresponding timing diagram for time allocation was shown. The overall simulation result shows the SNDR is 46.73dB, ENOB=7.47 bits with the sampling frequency of 3.81 GS/s, 57.54 mW power dissipation the achieved FoM is 41.99 J/conv-step.. This design was fabricated in 65-nm CMOS technology. A comparison with two other SAR ADC designs is shown in Figure 6.1. The figure shows that the FOM is the lowest compare with the other three and has a relative high SNDR. This means the ADC target the performance.

Specifications	ISSCC2012[1]	ISSCC2014[2]	ISSCC2015[3]	This Work
Architecture	SAR,TI	SAR,TI	SAR,TI	SAR
Technology	28nm UTBB FDSOI	32	65	28
Supply Voltage(V)	1	1.2	1.2	1
Sampling Rate(GS/s)	10	90	5	8
Resolution(bit)	6	8	6	8
SNDR(dB)	33.8	36	30.73	46.73
FOM(fJ/Conv.-step)	81	144	67.37	41.99
Power(mW)	32	667	10.6	57.54

Figure 6.1. Comparison table with two other SAR ADC designs

References

[1] Le Tual, S., et al., "22.3 A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI technology," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International* , vol., no., pp.382-383, 9-13 Feb. 2014

[2] Kull, L., et al., "22.1 A 90GS/s 8b 667mW 64× interleaved SAR ADC in 32nm digital SOI CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International* , vol., no., pp.378- 379, 9-13 Feb. 2014

[3] C. H. Chan, Y. Zhu, S. W. Sin, U. Seng-Pan and R. P. Martins, "26.5 A 5.5mW 6b 5GS/S 4×-lnterleaved 3b/cycle SAR ADC in 65nm CMOS," *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015, pp. 1-3