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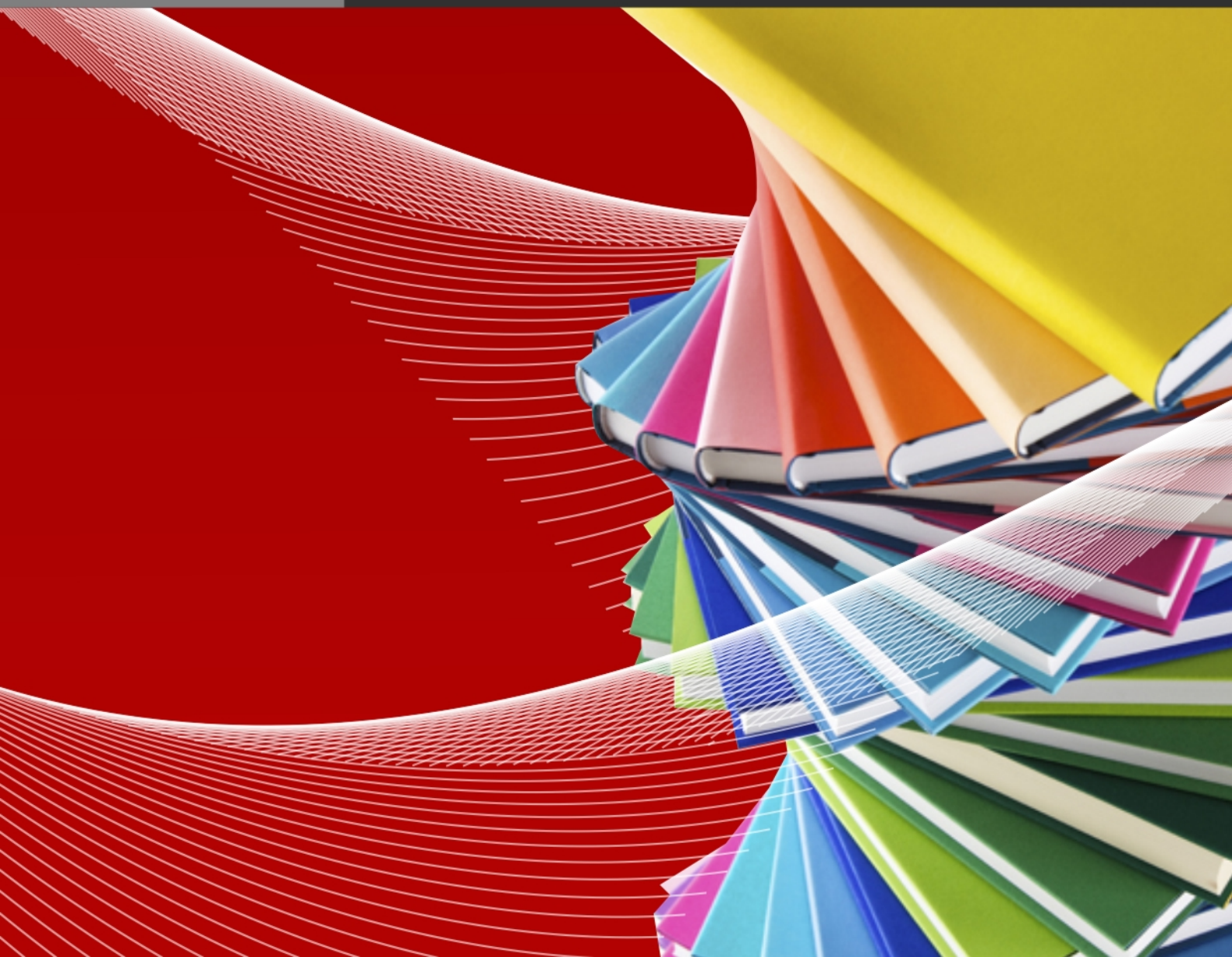

Electromagnetic Interference Resisting Circuit

by

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of the requirements for the Degree of

Bachelor of Science in Electrical and Electronics Engineering

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Faculty of Science and Technology

University of Macau

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Abstract

An electromagnetic interference (EMI) resisting circuit is described. It is improved from the classic Kuijk Bandgap with a PMOS pass device and an active load (PPDAL). Developed in 65 nm CMOS, the desired low reference voltage (441.3 mV) is achieved by substituting the BJT with MOSFET having a temperature coefficient (TC) of 10.65ppm/ ^{o}C. The EMI resisting ability in terms of DC shift is up to 2V amplitude by applying a double differential-input pair and a power supply independent bias scheme. The total power consumption is 104μW.

Contents

1. Introduction

1.1 Electromagnetic interference

Environmental electromagnetic pollution has drastically increased over the last decades. The omnipresence of wireless communication systems, new and various electronic appliances and the use of ever increasing frequencies, all contribute to a noisy electromagnetic environment which acts detrimentally on sensitive electronic equipment. It includes nearly all electronic areas, Owing to the growing use of electronic equipment and the ever increasing integration of different systems in the same product as well as in the same environment.[1]

Electromagnetic interference (or EMI, also called radio-frequency interference or RFI when in radio frequency) is disturbance that affects an electrical circuit due to either electromagnetic induction or electromagnetic radiation emitted from an external source. Since with the rapid development in modern technology, the voltage supply is scaling down, thus the disturbance may easily interrupt, obstruct, or otherwise degrade or limit the effective performance of the circuit.

EMI is typically picked up by cables or PCB components and conducted into the chip via package pins. Power supply external is really serious. When different circuits and systems are densely integrated in the same appliance, the parasitic electromagnetic coupling between these circuits sharing the same printed circuit board (PCB), power supply and ground lines, is indeed a critical design parameter that can no longer be safely excluded from a product design flow. How to solve EMI based on IC level becomes a serious problem, thus electromagnetic compatibility of integrated circuits is rising to be a hot topic.

1.2 Bandgap voltage reference

Bandgap voltage references (BVR) are circuits that provide a temperature and supply insensitive output voltage. It is a quite important building block in IC design. It can be used on ADCs and DACs. The reference voltage that the bandgap produces becomes critical to all other blocks performances. There are many types of state-of-the art designs. Bandgap voltage reference, which was firstly proposed by Widlar and war further developed by Kuijk and Brokaw. Nowadays almost all the bandgap designs are mainly based on them. Followed by one rule, which can provide a predictable reference voltage, possible low voltage and low temperature dependence.[2]

The disadvantage of these bandgaps is that an external resistive load would affect the output of the reference and its temperature characteristics. One solution is to add an output buffer. However, because of the limitation of the buffer, it's difficult for the reference to get a high PSRR. And it is not sensitive to resistive load, and because the output of the reference is located in a negative feedback loop, this structure is suitable for the design of the reference of high PSRR. However, it is hard for Kujik bandgap to introduce a current for secondary temperature compensation in standard CMOS technology, thus traditional Kujik bandgap has a poor temperature characteristic, normally larger than $20(\mathrm{ppm}/{}^{o}\mathrm{C})$. Voltage reference presented in this paper is based on Kujik bandgap.[3]

1.2.1 Classification of designing bandgap reference

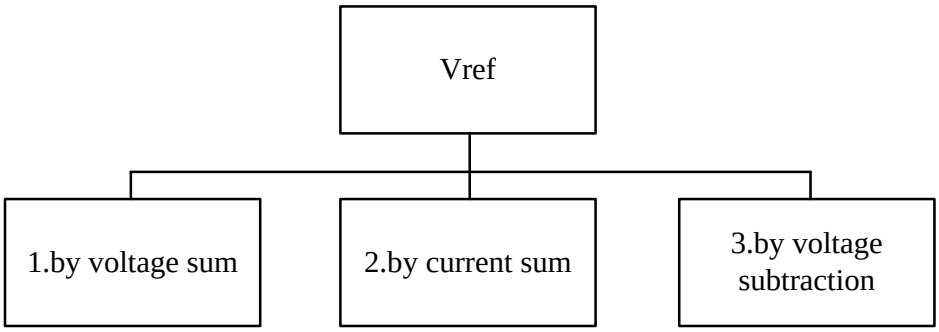

Figure 1.2.1 The classification of designing bandgap reference

Basically, bandgap is designed by the three kinds to produce the desired reference voltage:

1. By voltage sum: One is to directly generate the reference voltage by the summation of negative and positive voltages.

$$V_{ref} = \alpha \times V_{+} + \beta \times V_{-} \qquad \text{Eq.(1.2.1)}$$

$$V_{+}\left(\frac{\partial V}{\partial T} > 0\right), V_{-}\left(\frac{\partial V}{\partial T} < 0\right) \qquad \text{Eq.(1.2.2)}$$

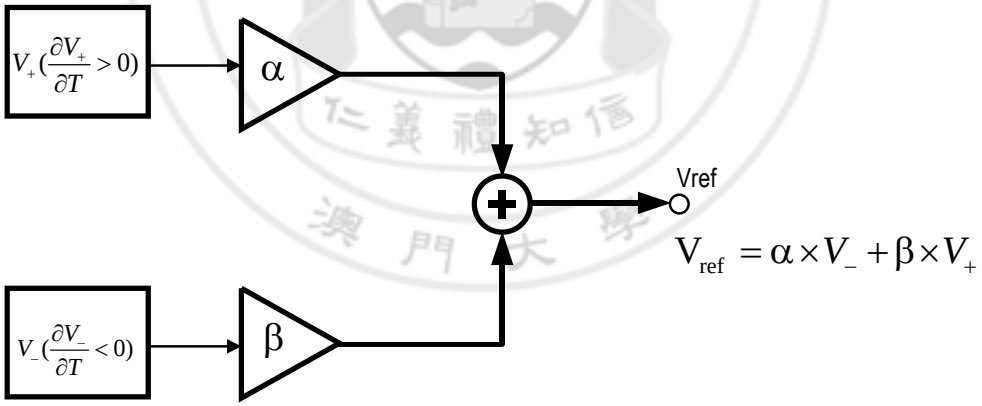

Figure 1.2.2 Bandgap reference by voltage sum

2. By current: Another is to generate the insensitive current first, and then by using current mirror applying on a resistor to have the reference voltage by

$$V_{ref} = \alpha \times V_{+} + \beta \times V_{-} \qquad \text{Eq.(1.2.3)}$$

$$I_{ref} = I_{CTAT} + I_{PTAT} \qquad \text{Eq.(1.2.4)}$$

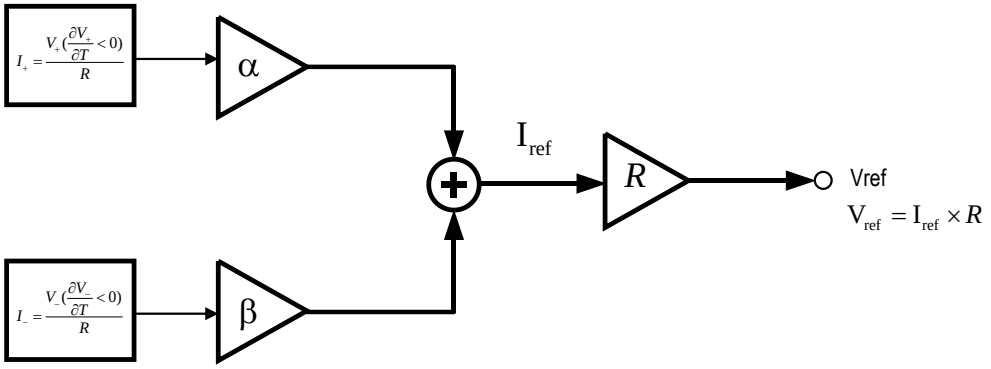

Figure 1.2.3 Bandgap reference by current

3. By voltage subtraction: There is still another way to get the insensitive voltage in subthreshould region of CMOS by finding the relationship between V_{GS} and V_{TH} with V_T, using the difference between gate-source voltages in an depletion process.[4]

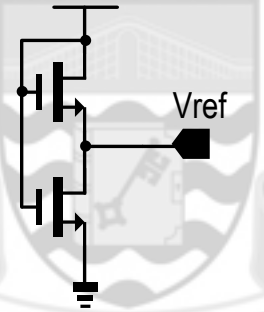

Figure 1.2.4 Bandgap reference by voltage subtraction

1.2.2 Kuijk bandgap reference

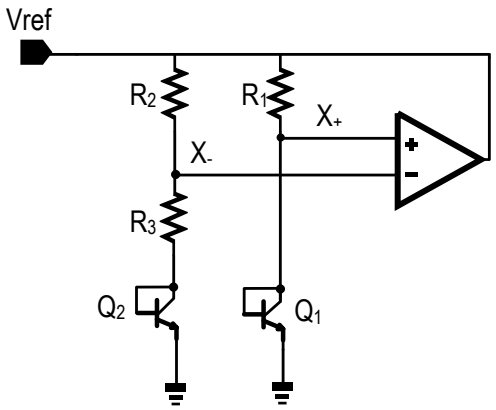

Figure 1.2.5 Kuijk bandgap reference

In BJT, V_{BE} is complementary proportional to absolute temperature (CPAT) which is obtained from the voltage across a forward biased p–n junction or the base-emitter voltage (V_{BE}) of a diode connected, while under different current passing through, ΔV_{BE} is proportional to absolute temperature (PTAT) which is generated by taking the difference in the base-emitter voltages of two BJT.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T l_n \qquad \text{Eq.(1.2.5)}$$

$$V_T = \frac{kT}{q} \qquad \text{Eq.(1.2.6)}$$

Where k is the Boltzmann constant, q is the electron charge and T is the temperature.

$$V_{ref} = \alpha \times V_{BE} + \beta \times \Delta V_{BE} \qquad \text{Eq.(1.2.7)}$$

$$V_{ref} = \alpha \times V_{BE} + \beta \times V_T l_n \qquad \text{Eq.(1.2.8)}$$

The temperature coefficient is quite an important characteristic for bandgap to determine its stability under different temperature, the equation is shown below:

$$TC = \frac{V_{max} - V_{min}}{V_{ref} \times (T_{max} - T_{min})} (ppm/\,^{o}C) \qquad \text{Eq.(1.2.9)}$$

It can be found that the smaller value of the Temperature coefficient, the better independency on temperature change.

1.2.3 Change BJT to MOSFET

In this circuit design, the BJT is changed to MOSFET. Thus, the voltage sum at zero Kelven will not be restricted to around 1.2V.

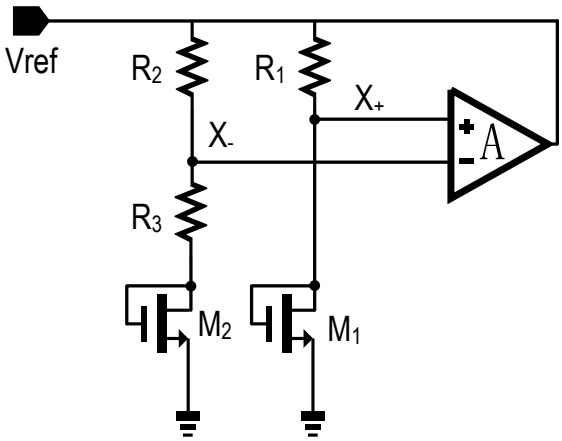

Figure 1.2.6 Kuijk bandgap reference in CMOS

It has some advantages that compare to BJT, the power supply can be lower. It can take less area and the reference voltage will no longer only be around 1.2V. Thus the NMOS width and length should have a large ratio in order to let it have bipolar transistor characteristics. However, the drawback is that the temperature coefficient will not perform as well as the BJT does. Since it is in subthreshold region, it can find that when drain-source voltage V_{DS} higher than 0.1 V, the subthreshold current can be expressed as:

$$I=I_0\exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \qquad \text{Eq.(1.2.10)}$$

Where

$$I_0=(W/L)\mu C_O x V_T^2(\eta-1) \qquad \text{Eq.(1.2.11)}$$

is the pre-exponential factor of the subthreshold current, then it can deduce that[5]

$$V_{gs}=V_{th}+nV_T\left(\ln C-\ln\frac{W}{L}+(\gamma-2)\ln T\right) \qquad \text{Eq.(1.2.12)}$$

Where n and γ are constants related to process of MOSFET, and C is related to the current of MOSFET in subthreshold region.

$$\Delta V_{gs}=V_{gs1}-V_{gs2}=nV_T\ln\frac{(W/L)_2}{(W/L)_1} \qquad \text{Eq.(1.2.13)}$$

Apparently, if $(W/L)_2>(W/L)_1$, the first order derivative of the difference voltage value is positive.

The current passes through R_2 is

$$I_2 = \frac{\Delta V_{gs}}{R_3} = \frac{nV_T}{R_3} \ln \frac{(W/L)_2}{(W/L)_1} \quad \text{Eq.(1.2.14)}$$

Then the reference voltage

$$V_{ref} = V_{gs2} + I_2 \times (R_2 + R_3) = V_{gs2} + nV_T \ln \frac{(W/L)_2}{(W/L)_1} \frac{R_2 + R_3}{R_3} \quad \text{Eq.(1.2.15)}$$

Through properly choose the size and the resistor value can get the reference voltage:

$$V_{ref} = \alpha \times V_+ + \beta \times V_- \quad \text{Eq.(1.2.16)}$$

$$V_+ \left(\frac{\partial V_T}{\partial T} > 0\right), V_- \left(\frac{\partial V_{gs2}}{\partial T} < 0\right) \quad \text{Eq.(1.2.17)}$$

$$\frac{\partial V_{ref}}{\partial V_T} = 0 \quad \text{Eq.(1.2.18)}$$

From above analysis, it solves the temperature coefficient problem, since this only focuses on the first-order compensation analysis. To be precisely let the reference voltage out of temperature drift, such as second-order and exponential-compensated optimization procedures can be applied.[5]

2. EMI-resisting Bandgap

From now on, analysis from how to resist EMI is based on bandgap from small signal analysis and large signal analysis. For small signal analysis, concentrate on gain, higher PSRR. For large signal analysis, focus on bias problem which is related to DC shift, how large the interference amplitude the circuit can sustain.

For interferences with different frequencies, the bandwidth is limited. If the frequency is within the bandwidth, the interference will be attenuated by the loop gain. If the frequency is out of the bandwidth range, the interference will be filtered out by RC filter as well as by optional capacitors decoupling the power supply. The NPD, PPD and PPDAL in 'EMC of Analog Integrated Circuits'[6] will be discussed.

2.1 NPD

NPD refers to NMOS pass device, the original one OTA in Kuijk bangap following a NMOS transistor in a source follower configuration in order to keep the subsequent EMI analysis compact. The circuit is depicted below:

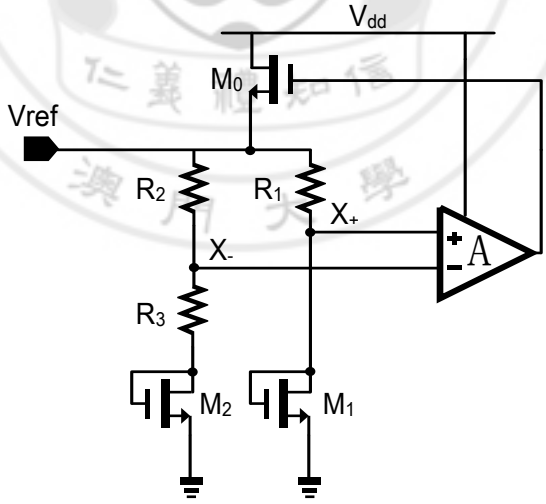

Figure 2.1.1 The NPD Kuijk bandgap

2.1.1 Small signal analysis

If the EMI signal is quite small, taking the small signal analysis into consideration. When frequency becomes higher, some important parasitic capacitances should be included, it will do affect the circuit. The schematic diagram is drawn below to analyze:

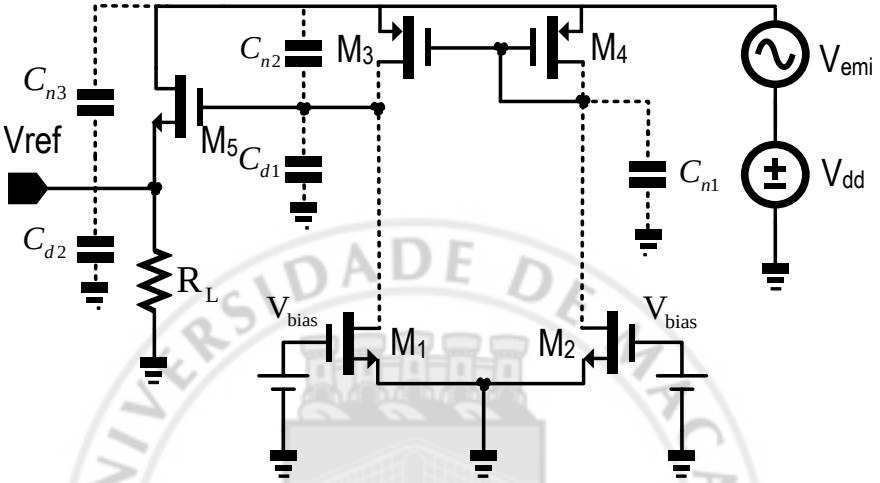

Figure 2.1.2 The full NPD Kuijk bandgap

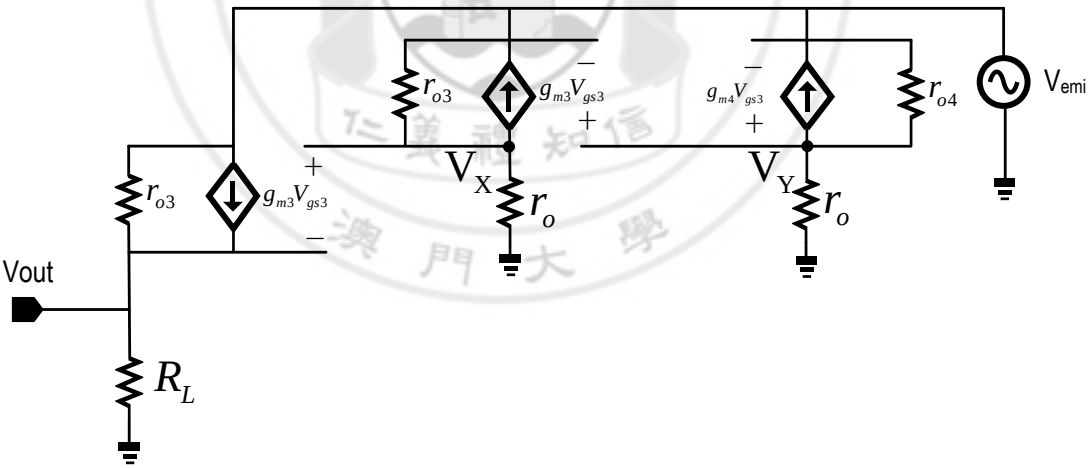

Figure 2.1.3 The small signal circuit of NPD kuijk bandgap

Using KCL, set equations to analysis the small signal model below:

$$\frac{V_Y}{r_o}+g_m(V_Y-V_{in})+\frac{V_Y-V_{in}}{r_o}=0 \qquad \text{Eq.(2.1.1)}$$

$$\frac{V_X}{r_o}+g_m(V_Y-V_{in})+\frac{V_X-V_{in}}{r_o}=0 \qquad \text{Eq.(2.1.2)}$$

$$\frac{V_{out}}{R_L} = \frac{V_{in}-V_{out}}{r_o} + g_m(V_X - V_{out}) \quad \text{Eq.(2.1.3)}$$

From Eq.(2.1.1)

$$V_Y = \frac{1+g_m r_o}{2+g_m r_o} V_{in} \quad \text{Eq.(2.1.4)}$$

From Eq.(2.1.2)

$$V_X \approx \frac{1+g_m r_o}{2+g_m r_o} V_{in} \quad \text{Eq.(2.1.5)}$$

V_X and V_Y two nodes are similar to equal voltages to Vin, it doesn't deteriorate the EMI signal. The C_{d1} can help to eliminate EMI at high frequency range.

Thus

$$(g_m + \frac{r_o + R_L}{r_o R_L}) V_{out} = \frac{V_{in}}{r_o} + \frac{(1+g_m r_o)}{2+g_m r_o} V_{in} \quad \text{Eq.(2.1.6)}$$

$$V_{out} \approx \frac{g_m R_L}{1+g_m R_L} V_{in} \quad \text{Eq.(2.1.7)}$$

So the gain from the EMI source to reference voltage is

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m R_L}{1+g_m R_L} \quad \text{Eq.(2.1.8)}$$

For this equation, in order to minimize the effect of EMI, $g_m R_L$ should be as small as possible, better to approach 0. However, it is quite hard to realize it, thus to control the value of R_L as small as possible as well as the g_m. g_m is the transconductance which relates to the current, the size and the overdrive voltage. Different situation g_m is determined by different parameters. Since overdrive voltage is always constant, thus

$$g_m = \sqrt{2 I_d u_n C_{ox} \frac{W}{L}} \quad \text{Eq.(2.1.9)}$$

which is proportional to I_d and W/L.

For high frequencies, it needs to consider the parasitic capacitances of each MOSFET. Thus it can be analyzed it in detail by using miller compensation.

$$C_{n1}=C_{DB4}+C_{DB2}+C_{GD2}+C_{GD4} \quad \text{Eq.(2.1.10)}$$

$$C_{d2}=C_L+C_{GS5}(1-\frac{g_m R_L+1}{g_m R_L}) \quad \text{Eq.(2.1.11)}$$

$$C_{n3}=C_{GD5}+C_{GS5} \quad \text{Eq.(2.1.12)}$$

$$\frac{V_Y}{r_o}+g_m(V_Y-V_{in})+\frac{V_Y-V_{in}}{r_o}=0 \quad \text{Eq.(2.1.13)}$$

$$\frac{V_X}{r_o}+\frac{V_X}{SC_{d1}}+g_m(V_Y-V_{in})+\frac{V_X-V_{in}}{r_o}=0 \quad \text{Eq.(2.1.14)}$$

$$\frac{V_{out}}{R_L}+\frac{V_{out}}{SC_{d2}}=\frac{V_{in}-V_{out}}{r_o}+g_m(V_X-V_{out})+\frac{V_{in}-V_{out}}{SC_{n3}} \quad \text{Eq.(2.1.15)}$$

$$\frac{V_{out}}{V_{in}}\approx\frac{g_m R_L}{1+g_m R_L}\times\frac{(SC_{n3}r_o+1)(2g_m+SC_{d1})}{(2+SC_{d1}r_o)(SC_{d2}+\frac{R_L}{R_L+1/g_m})} \quad \text{Eq.(2.1.16)}$$

So it can find that

$$\omega_{p1}=\frac{2}{C_{d1}r_o},\ \omega_{p2}=\frac{g_m R_L+1}{C_{d2}R_L},\ \omega_{z1}=\frac{1}{C_{n3}r_o},\ \omega_{z2}=\frac{2g_m}{C_{d1}} \quad \text{Eq.(2.1.17)}$$

Other poles and zeros since they are quite far away from the dominant poles and zeors, so don't need to consider such as $\omega_{p2}=\frac{g_{m4}}{C_{n1}}$. Since directly from the circuit diagram easily find the poles and zeros directly. To follow the rule that $\omega=\frac{1}{RC}$. Poles are that RC coupled to the ground while zeros are almost formed by floating RC paths.

ω_{p1} is located at the gate of M5, looking at this node,

$$R=r_0 \parallel r_0=\frac{r_o}{2},\ C=C_{d1},\ \text{so}\ \ \omega_{p1}=\frac{2}{C_{d1}r_o} \quad \text{Eq.(2.1.18)}$$

ω_{p2} is located at the output, the source of M5,

$$R=R_L \parallel \frac{1}{g_m},\ C=C_{d2}.\ \text{So}\ \ \omega_{p2}=\frac{g_m R_L+1}{C_{d2}R_L} \quad \text{Eq.(2.1.19)}$$

Try to minimize the ω_{p1} and ω_{p2} to increase the PSRR at DC frequency range, one is to increase the MOSFET length and another is to increase the capacitance of C_{d2}. For zeros, it needs to find the paths which the signal passes. ω_{z1} is formed by the drain of M5 to the source of M5, thus

$$R=r_0,\ \text{while}\ \ C=C_{n3},\ \text{thus}\ \ \omega_{z1}=\frac{1}{C_{n3}r_o} \qquad \text{Eq.(2.1.20)}$$

The second path is passing through the source of M3 and then to the gate of M5, finally from the gate of M5 to the output. This one need to be calculated that

$$\omega_{z2}=\frac{2g_m}{C_{d1}} \qquad \text{Eq.(2.1.21)}$$

2.1.2 Large signal analysis

Without considering channel length modulation,

$$I_{d1-no}EMI=\frac{1}{2}uC_{ox}\frac{W}{L}(V_{GS1}\text{-}V_{TH})^2=I_{d3-no}EMI=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{SG3}\text{-}|V_{TH}|)^2$$

Eq.(2.1.22)

$$I_{d1-with}EMI=I_{d3-with}EMI=\lim_{T\to\infty}\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}}I_{d1}(t)dt=\overline{\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{SG3}+v_{sg3}\text{-}|V_{TH}|)^2}$$

Eq.(2.1.23)

Since considering the electromagnetic interference as a sinusoidal signal, its sum within one period is zero. So that adding the EMI signal, the current will be:

$$I_{d1-with}EMI=I_{do-with}EMI+\overline{\frac{1}{2}\mu C_{ox}\frac{W}{L}(v_{sg3})^2} \qquad \text{Eq.(2.1.24)}$$

The average current of I_{d1} is increased, thus its drain voltage will increase too thus force the gate voltage of M5 to a higher value. The output voltage is followed by a source follower and thus it will change by the change of V_{G5}.

More specifically, separately analyze EMI for positive and negative cycles each. For positive cycle values of EMI, both of M1 and M2 are in saturation. The large signal output resistance of them which defined as the ratio of mean drain-source

voltage (V_{dsi}) to the mean drain current (I_{di}) will decrease. M1 will be affected more than M2 since M4 is diode connected, EMI can pass through and the mean value of drain voltage of M2 can be almost eliminated. For negative cycle of EMI swing, both of M1 and M2 are easily forced into linear triode region if EMI signal is relatively large since drain voltage is not high enough. Conversely, the large signal output resistance will increase. The tail current will be kept the same, thus the average drain current I_{d1} will steadily decrease and I_{d2} increases by the same amount. V_{G5} will decrease also so as reference voltage.

However EMI injected problem is not solved for M5, since its gate source voltage V_{GS} can't maintain a constant value.

2.2 PPD

PPD refers to PMOS pass device topology. Compares to NPD, it replaces the NMOS Mo to PMOS, compensation capacitance C_{d1} is connected between the gate and source of PMOS. It has a constant gate-source voltage and a constant current as well. Owing to this replacement, EMI coupling has been decreased. The OTA keeps the same. The circuit is depicted below:

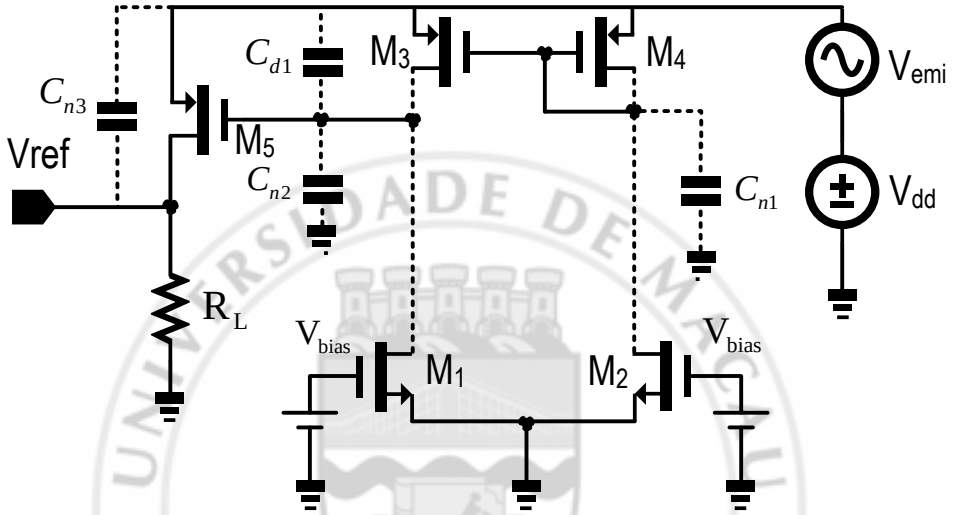

Figure 2.2.1 The PPD kuijk bandgap circuit

2.2.1 Small signal analysis

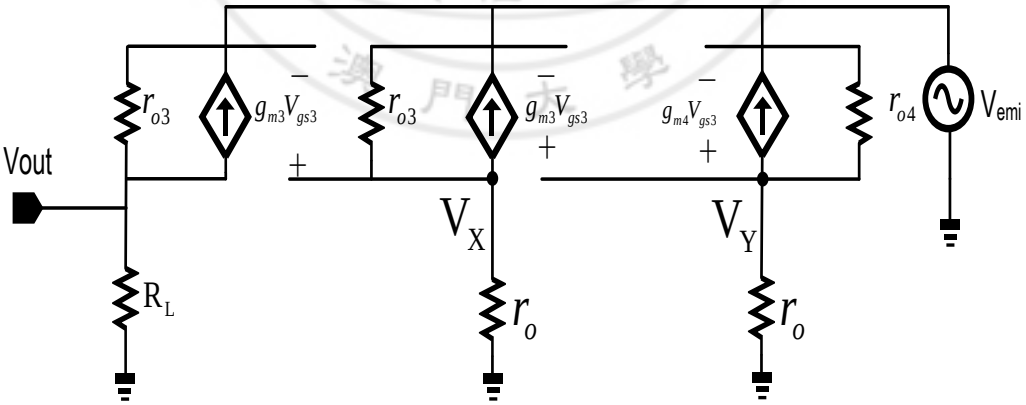

Figure 2.2.2 The small signal circuit of PPD Kuijk bandgap

Set up equations for the small signal model of PPD. The PSRR is calculated below by KCL. Assume all of the drain source resistances for each MOSFET are equal.

$$\frac{V_Y}{r_o}+g_m(V_Y-V_{in})+\frac{V_Y-V_{in}}{r_o}=0 \qquad \text{Eq.(2.2.1)}$$

$$\frac{V_X}{r_o}+g_m(V_Y-V_{in})+\frac{V_X-V_{in}}{r_o}=0 \qquad \text{Eq.(2.2.2)}$$

$$\frac{V_{out}}{R_L}+\frac{V_{out}-V_{in}}{r_o}+g_m(V_X-V_{in})=0 \qquad \text{Eq.(2.2.3)}$$

From Eq.(2.2.1)

$$V_Y=\frac{1+g_m r_o}{2+g_m r_o}V_{in} \qquad \text{Eq.(2.2.4)}$$

From Eq.(2.2.2)

$$V_X \approx \frac{1+g_m r_o}{2+g_m r_o}V_{in} \qquad \text{Eq.(2.2.5)}$$

Since the OTA doesn't change, the two node voltages will keep the same nearly equal to Vin.

Thus

$$\frac{r_o+R_L}{r_o R_L}V_{out}=\frac{V_{in}}{r_o}+\frac{g_m}{2+g_m r_o}V_{in} \qquad \text{Eq.(2.2.6)}$$

$$V_{out} \approx \frac{2R_L}{r_o+R_L}V_{in} \qquad \text{Eq.(2.2.7)}$$

So the gain from the EMI source to reference voltage is

$$\frac{V_{out}}{V_{in}} \approx \frac{2R_L}{r_o} \qquad \text{Eq.(2.2.8)}$$

For PPD, the replacing PMOS has changed the PSRR higher than the NMOS, it determines the final PSRR. The PSRR which is related to the output resistance R_L and r_o. To minimize the EMI effect, it can reduce the loading resistance R_L as well as to increase r_o. r_o is due to the channel length modulation which is proportion to the length of MOSFET, the PMOS M5. The longer the length the corresponding resistance is increased. Thus it can have a higher attenuation for EMI signal.

Just do as the NPD does, for high frequencies:

$$C_{n2}=C_{DB3}+C_{DB1}+C_{GD1}+C_{DG3}+C_{GS3}(1+g_mR_L) \quad \text{Eq.(2.2.9)}$$

$$C_{d2}=C_L+C_{GD5}(1+\frac{1}{g_mR_L}) \quad \text{Eq.(2.2.10)}$$

$$C_{n3}=C_{GD5}+C_{GS5} \quad \text{Eq.(2.2.11)}$$

For ω_{p1} and ω_{z1}, there are no changes so

$$\omega_{p1}=\frac{2}{C_{d1}r_o} \quad \text{Eq.(2.2.12)}$$

and

$$\omega_{z1}=\frac{1}{C_{n3}r_o} \quad \text{Eq.(2.2.13)}$$

Since NMOS has been replaced by PMOS, ω_{p2} and ω_{z2} will change. For ω_{p2}, its output resistance has changed into

$$r_o \parallel R_L \approx R_L \quad \text{Eq.(2.2.14)}$$

$$\omega_{p2}=\frac{1}{C_{d2}R_L} \quad \text{Eq.(2.2.15)}$$

Same reason

$$\omega_{z2}=\frac{4}{C_{d1}r_o} \quad \text{Eq.(2.2.16)}$$

So the gain from the EMI source to reference voltage is

$$\frac{V_{out}}{V_{in}} \approx \frac{2R_L}{r_o} \times \frac{(SC_{n3}r_o+1)(1+SC_{d1}r_o/4)}{(2+SC_{d1}r_o)(SC_{d2}R_L+1)} \quad \text{Eq.(2.2.17)}$$

To this equation, ω_{z2} can be set as large as possible, thus it locates far away from the second pole which can prolong the main pole effect to degrade the EMI effect. ω_{p2} can be set at a small value to degrade the EMI signal in a lower frequency range. Just like miller effect so that it can decrease the loading resistance R_L. Since all of the other simulation works are based on PPD, so the simulation results are shown below:

The PSRR simulation result from reference node to EMI source is shown below:

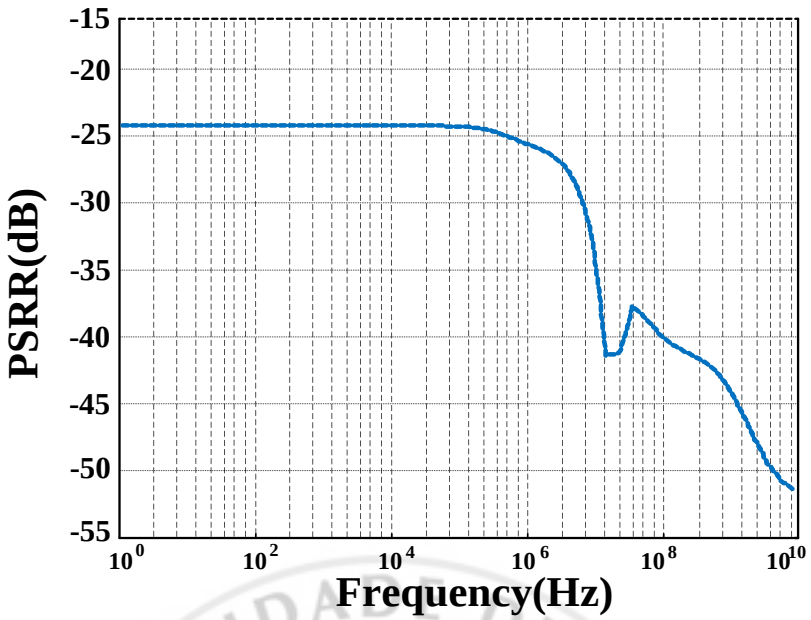

Figure 2.2.5 The PSRR simulation result from 1Hz to 10GHz

It basically reflects the transfer function, the difference is due to the simulation result is closed loop and the transfer function is open loop. For more detail analysis, it will be discussed later.

The following figures show the reference voltage and its temperature coefficient:

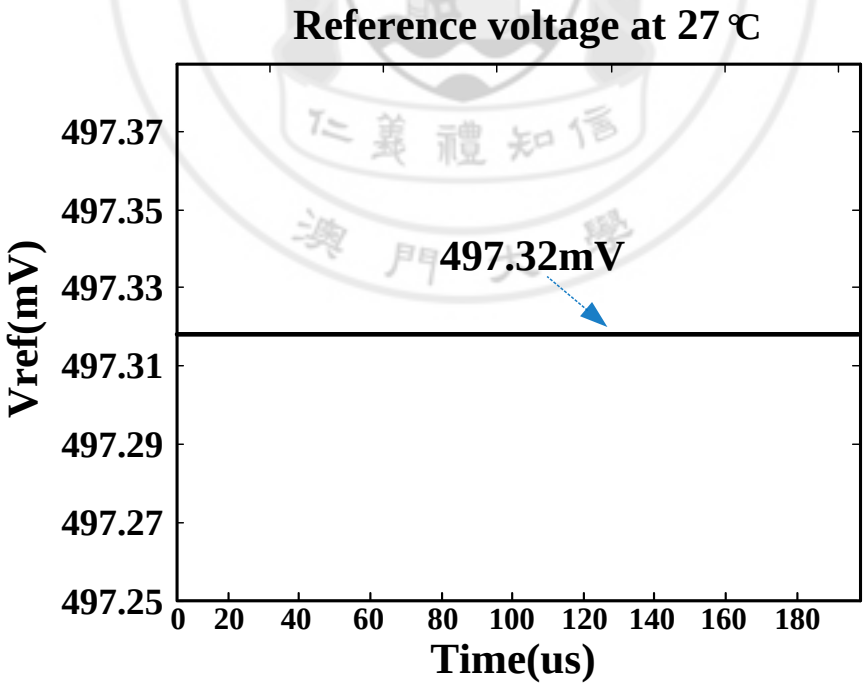

Figure 2.2.6 The reference output voltage at 27℃

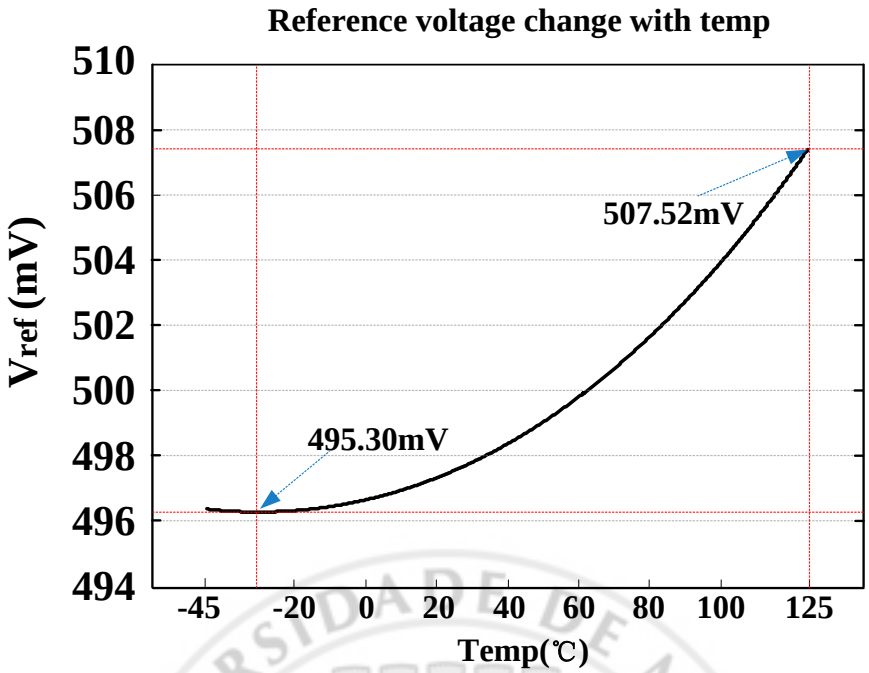

Figure 2.2.7 Reference voltage change from -45 ℃ to 125 ℃

The temperature sweep range is from -45 ℃ to 125 ℃. The temperature coefficient is shown below:

$$T = \frac{V_{max}-V_{min}}{V_{ref}\times(T_{max}-T_{min})} = \frac{507.52mV-495.3mV}{497.32mV\times(125+45)} \approx 144.5(ppm/\ ^{o}C) \quad \text{Eq.(2.2.18)}$$

At last, the total power consummation is

$$P = UI = 1.2V \times 307.9u = 369.5\mu W \quad \text{Eq.(2.2.19)}$$

2.2.2 Large signal analysis

Compare it to NPD, it has an improvement that replace the NMOS pass transistor M5 by a PMOS transistor. A capacitor Cd is connected between its gate and source of M5. Others remain the same. The effect of capacitor Cd is to couple the EMI signal to the gate of M5 when it's in a frequency domain. In this way, M5 has a constant gate-source voltage.

$$I_{d5-no}EMI = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{SG5}-|V_{TH}|)^2 \quad \text{Eq.(2.2.20)}$$

$$I_{d5-with}EMI = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{S5}+V_{emi}-(V_{G5}+V_{emi})-|V_{TH}|)^2 = I_{d5-no}EMI \quad \text{Eq.(2.2.21)}$$

So, EMI is reduced at output when it is in low frequency domain. However, at higher frequencies, due to the parasitic capacitance effect of M5, C_{gd} , C_{gs} and C_{db} will cause a voltage division of EMI. Thus EMI is not perfectly reduced at V_{GS}. Morever, EMI signal will also couples from the gate of M5 to OTA. Thus, EMI will cause a voltage fluctuation for drain voltage for M1 and M2. It will also be disturbed. This problem is not solved compared to NPD as well.

2.3 PPDAL

Among NPD, PPD and PPDAL, PPDAL has the best performance to have largest gain, smallest DC shift and also maximum EMI sustain ability. Therefore, choosing PPDAL to analysis and improve. PPDAL refers to PMOS pass device with active load. Compare to PPD, It adds one more current mirror M6-M7 above at the drain of input pair M1-M2. This has some improvements also in small signal as well as in large signal aspects. The circuit is depicted below:

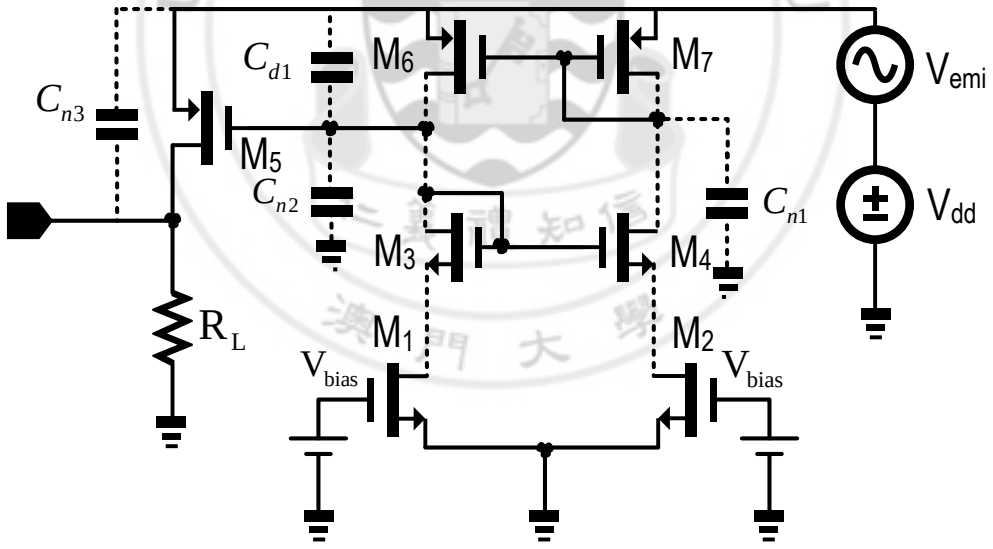

Figure 2.3.1 The PPDAL kuijk bandgap circuit

2.3.1 Small signal analysis

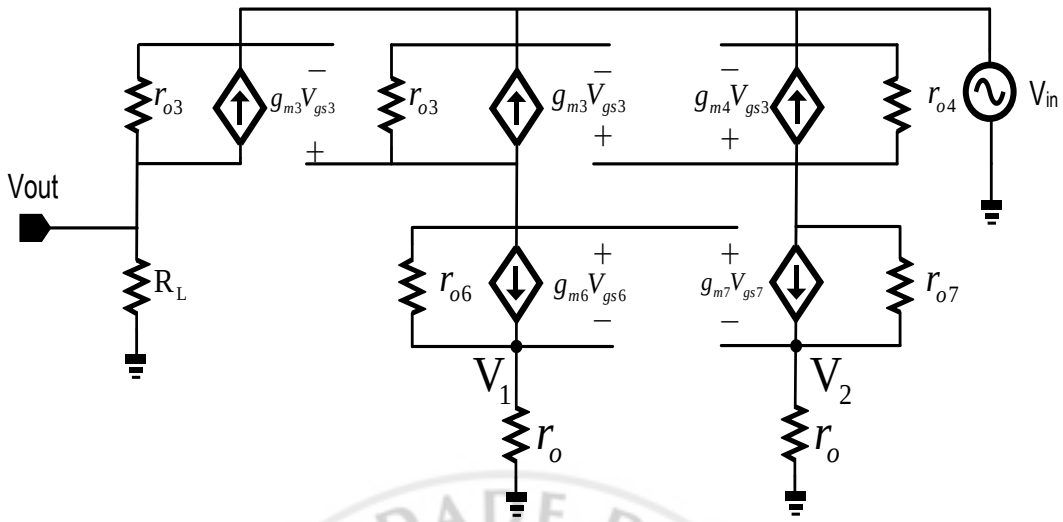

Figure 2.3.2 The small signal diagram of Kuijk bandgap circuit

According to the small signal model, it can set up equations to solve the gain problem. The PSRR is calculated below:

$$\frac{V_{g3}-V_{in}}{r_o}+g_m(V_{g3}-V_{in})+\frac{V_{g3}-V_2}{r_o}+g_m(V_X-V_2)=0 \qquad \text{Eq.(2.3.1)}$$

$$\frac{V_{g3}-V_2}{r_o}+g_m(V_X-V_2)=\frac{V_2}{r_o} \qquad \text{Eq.(2.3.2)}$$

$$\frac{V_x-V_{in}}{r_o}+g_m(V_{g3}-V_{in})+\frac{V_x-V_1}{r_o}+g_m(V_X-V_1)=0 \qquad \text{Eq.(2.3.3)}$$

$$\frac{V_x-V_1}{r_o}+g_m(V_X-V_1)=\frac{V_1}{r_o} \qquad \text{Eq.(2.3.4)}$$

$$\frac{V_{out}}{R_L}+\frac{V_{out}-V_{in}}{r_o}+g_m(V_X-V_{in})=0 \qquad \text{Eq.(2.3.5)}$$

From Eq.(3.3.2)

$$V_2=\frac{V_{g3}+g_m r_o V_x}{2+g_m r_o} \qquad \text{Eq.(2.3.6)}$$

From Eq.(3.3.4)

$$V_1=\frac{V_x+g_m r_o V_x}{2+g_m r_o} \qquad \text{Eq.(2.3.7)}$$

Thus From Eq.(2.3.1)

$$V_{g3}=\frac{g_m V_{in}+g_m{}^2 r_o V_{in}-g_m r_o V_x}{1+g_m+g_m{}^2 r_o} \qquad \text{Eq.(2.3.8)}$$

From Eq.(2.3.3)

$$g_m r_o V_{in}+2V_{in}+\frac{V_{in}}{g_m r_o}=g_m r_o V_x+2V_x+\frac{2V_x}{g_m r_o} \quad , V_x \approx V_{in} \qquad \text{Eq.(3.3.9)}$$

Thus from Eq.(2.3.5)

$$\frac{V_{out}}{V_{in}} \approx \frac{R_L}{r_o+R_L} \approx \frac{R_L}{r_o} \qquad \text{Eq.(2.3.10)}$$

For this structure, the PSRR is only related to loading resistance R_L and r_O, it is the smallest one compared to the other two. This is due to $R_L << r_O$, it can almost get the final PSRR. Know that the smaller R_L and the larger r_O results higher PSRR which can be realized by increasing the length of PMOS M5. In theoretically calculation, without some mismatches and keep the same parameter value, the PPDAL PSRR has a 20log2dB increase around 6dB better than PPD.

For high frequencies, parasitic capacitance is included as well:

$$C_{n2}=C_{DB3}+C_{DB6}+C_{DG3}(1+g_m r_o) \qquad \text{Eq.(2.3.11)}$$

$$C_{d2}=C_L+C_{GD5}(1+\frac{1}{g_m R_L}) \qquad \text{Eq.(2.3.12)}$$

$$C_{n3}=C_{GD5}+C_{GS5} \qquad \text{Eq.(2.3.13)}$$

Since only C_{n2} has changed due to the gain of the OTA has changed. Same as PPD, $\boldsymbol{\omega_{p1}}$ and $\boldsymbol{\omega_{z1}}$ has not changed,

$$\omega_{p2}=\frac{1}{C_{d2}R_L}, \omega_{z1}=\frac{1}{C_{n3}r_o} \qquad \text{Eq.(2.3.14)}$$

The impedance looking for ω_{p1} has changed due to the output impedance of the OTA changed from $r_o \| r_o \approx r_{03}$, this will analyze it later.

So

$$\omega_{p1} = \frac{1}{C_{d1} r_o} \qquad \text{Eq.(2.3.15)}$$

The same reason for ω_{z2}

$$\omega_{z2} = \frac{2}{C_{d1} r_o} \qquad \text{Eq.(2.3.16)}$$

So the gain from the EMI source to reference voltage is

$$\frac{V_{out}}{V_{in}} \approx \frac{R_L}{r_o} \times \frac{(SC_{n3} r_o + 1)(1 + SC_{d1} r_o / 2)}{(1 + SC_{d1} r_o)(SC_{d2} R_L + 1)} \qquad \text{Eq.(2.3.17)}$$

Since the pole is related to the output resistance. According to this structure, the OTA has changed, and to see the new structure influence to the OTA output, since the output resistance is related to the EMI resisting ability. To see whether the input pair drain source resistances affect the OTA resistance or not, so it needs to calculate the output resistance in small signal model and is shown below:

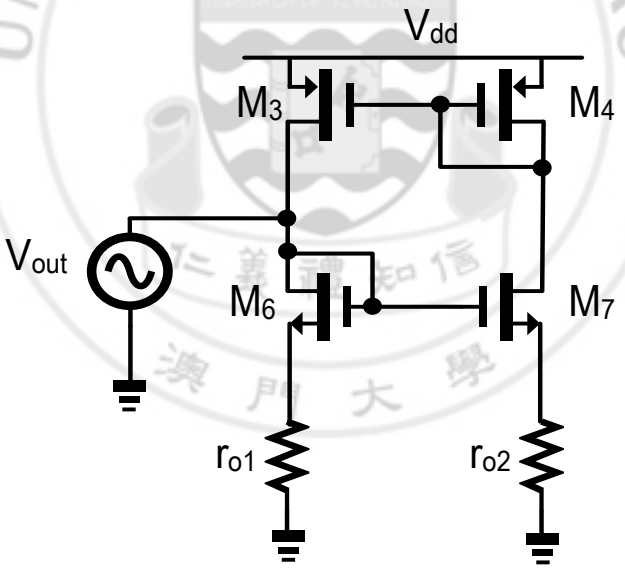

Figure 2.3.3 The simplify model of calculating R_{out}

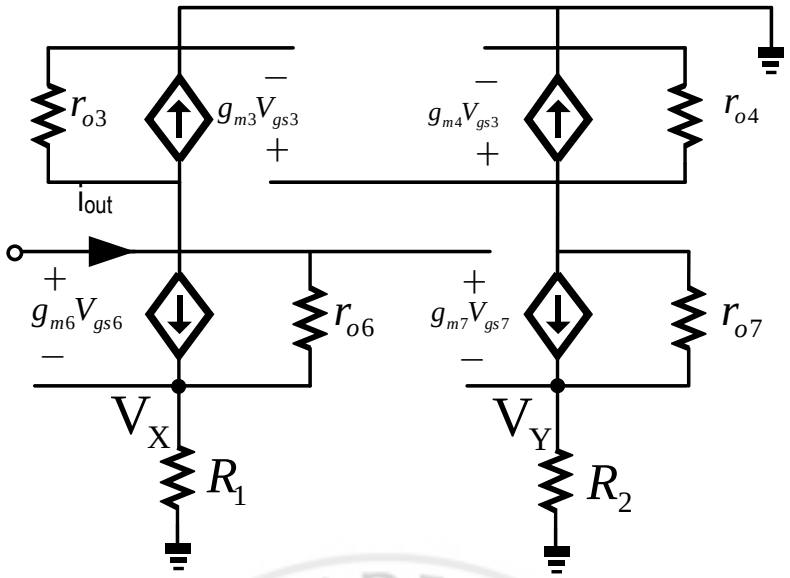

Figure 2.3.4 The small signal model for calculating R_{out}

Using KCL:

$$g_{m3}V_{gs3}+\frac{V_{out}}{r_{o3}}+\frac{V_x}{R_1}=0 \qquad \text{Eq.(2.3.18)}$$

$$\frac{V_{out}-V_X}{r_{o6}}+g_{m6}(V_{out}-V_X)=\frac{V_X}{R_1} \qquad \text{Eq.(2.3.19)}$$

From Eq.(2.3.19)

$$g_{m6}r_{o6}V_{out}+V_{out}=(\frac{r_{o6}}{R_1}+1+g_{m6}r_{o6})V_x \qquad \text{Eq.(2.3.20)}$$

Thus

$$V_{out}\approx V_X \qquad \text{Eq.(2.3.21)}$$

$$g_{m4}V_{gs3}+\frac{V_{gs3}}{r_{o4}}+\frac{V_Y}{R_2}=0 \qquad \text{Eq.(2.3.22)}$$

$$\frac{V_{gs3}-V_Y}{r_{o7}}+g_{m7}(V_{out}-V_Y)=\frac{V_Y}{R_2} \qquad \text{Eq.(2.3.23)}$$

$$V_Y=\frac{R_2V_{gs3}+g_{m7}r_{o7}R_2V_{out}}{g_{m7}r_{o7}R_2} \qquad \text{Eq.(2.3.24)}$$

$$I_{out}=\frac{V_x}{R_1}+\frac{V_{out}}{r_{o3}}+g_{m3}V_{gs3} \quad \text{Eq.(2.3.25)}$$

$$g_{m4}V_{gs3}+\frac{V_{gs3}}{r_{o4}}+\frac{R_2V_{gs3}+g_{m7}r_{o7}V_{out}}{g_{m7}r_{o7}R_2}=0 \quad \text{Eq.(2.3.26)}$$

Thus

$$V_{gs3}=-\frac{V_{out}}{g_{m4}R_2} \quad \text{Eq.(2.3.27)}$$

Finally

$$I_{out}=\frac{V_{out}}{R_1}+\frac{V_{out}}{r_{o3}}-\frac{V_{out}}{R_2} \quad \text{Eq.(2.3.28)}$$

The output resistance is

$$R_{out}=\frac{r_{o3}}{1+r_{o3}\times\frac{R_2-R_1}{R_1R_2}} \quad \text{Eq.(2.3.29)}$$

From output resistance, if R_1 and R_2 are equal or they just have a small mismatch, the final output resistance is about r_{o3}. The variation of the resistance of M1 and M2 are masked by the adding current mirror. The output resistance is independent of the resistance of M1 and M2. If there is some variation on the drain voltages of M1 and M2, it can't change the output resistance of OTA quite obviously. It is most relied on the output resistance of M3.

In order to calculate the overall loop gain, it needs to calculate the OTA, the circuit is depicted below:

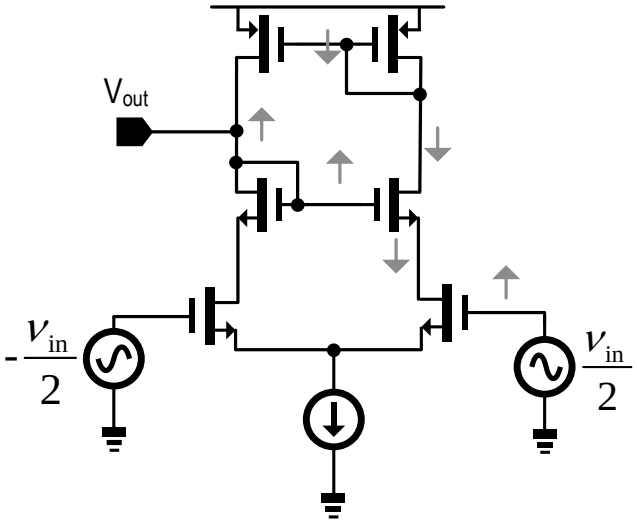

Figure 2.3.5 The OTA circuit in PPDAL

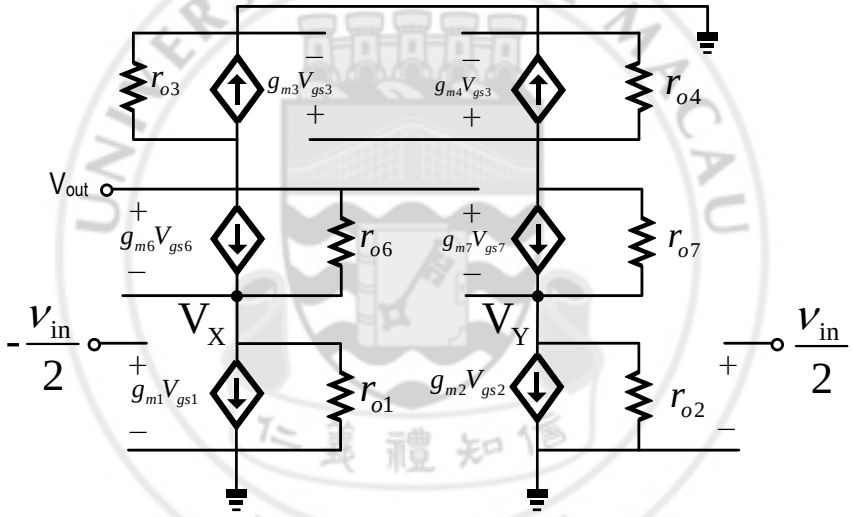

Figure 2.3.6 The small signal model of OTA

Thus set up KCL equations to solve the OTA gain:

$$\frac{V_{out}}{r_{o3}}+g_{m3}V_{gs3}+\frac{V_{out}-V_x}{r_{o6}}+g_{m6}(V_{out}-V_x)=0 \qquad \text{Eq.(2.3.30)}$$

$$\frac{V_{out}-V_x}{r_{o6}}+g_{m6}(V_{out}-V_x)=\frac{V_x}{r_{o6}}+g_{m1}(-\frac{V_{in}}{2}) \qquad \text{Eq.(2.3.31)}$$

$$\frac{V_{gs3}}{r_{o4}}+g_{m4}V_{gs4}+\frac{V_{gs3}-V_Y}{r_{o7}}+g_{m7}(V_{out}-V_Y)=0 \qquad \text{Eq.(2.3.32)}$$

$$\frac{V_{gs3}-V_Y}{r_{o7}}+g_{m7}(V_{out}-V_Y)=\frac{V_Y}{r_{o2}}+g_{m2}(\frac{V_{in}}{2}) \qquad \text{Eq.(3.3.33)}$$

From Eq.(2.3.31)

$$V_x \approx \frac{V_{out}}{g_{m6}r_{o6}} + V_{out} + \frac{g_{m1}V_{in}}{2g_{m6}} \quad \text{Eq.(2.3.34)}$$

From Eq.(2.3.33)

$$V_Y \approx \frac{V_{gs3}}{g_{m7}r_{o7}} + V_{out} - \frac{g_{m2}V_{in}}{2g_{m7}} \quad \text{Eq.(2.3.35)}$$

From Eq.(2.3.32)

$$V_{gs3} \approx -\frac{1}{r_{o2}}\left(\frac{g_{m2}V_{in}r_{o2}}{2} + V_{out} - \frac{g_{m2}V_{in}}{2g_{m7}}\right) \times \frac{r_{o4}}{1+g_{m4}r_{o4}} \quad \text{Eq.(2.3.36)}$$

Thus, the OTA gain is equal to

$$\frac{V_{out}}{V_{in}} = r_{o3}\left(g_{m1} - \frac{1}{r_{o1}}\right) = g_{m1}r_{o3} - 1 \approx g_{m1}r_{o3} \quad \text{Eq.(2.3.37)}$$

For this result, the OTA gain no longer be $g_{m1}\, r_{o3} \| r_{o1}$, it has increased to be $g_{m1}r_{o3}$. And the resistance is not related to the input differential pair, only depends on the length of M3. So adjust the length of M3 to increase the resistance of r_{o3} to increase the gain. However, the transconductance is also related to the differential pair. To increase the current I_d and the width of input W, in trade-off the power will be increased as well as the parasitic capacitances.

Since know that the OTA circuit contains positive feedback loop, if the gate voltage of M7 increases, the gate voltage of M3 and M4 decreases, and consequently, the gate voltage of M6 increases. This one will illustrate in the figure below:

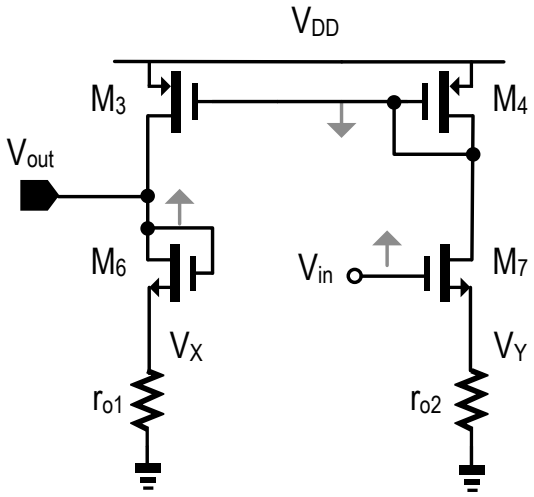

Figure 2.3.7 Active load positive feedback circuit

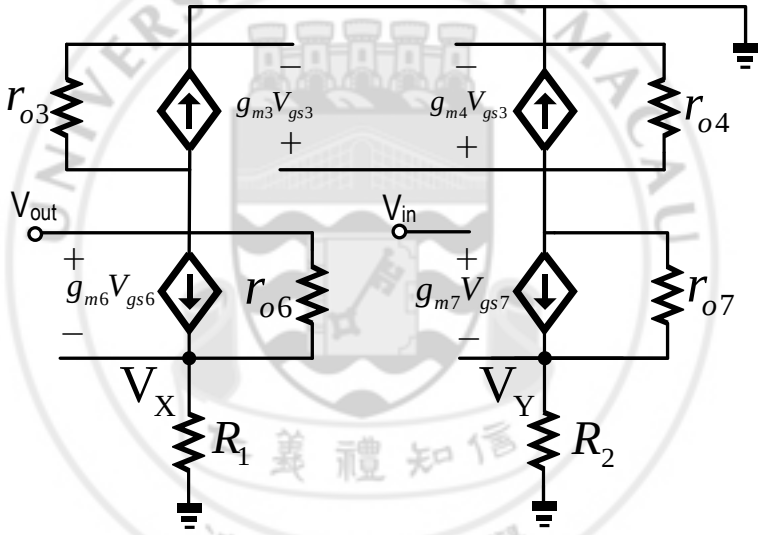

Figure 2.3.8 Small signal model for positive feedback

If it is the positive feedback loop, it is easily to be unstable. However, in this way, the loop gain is only let to be smaller than 1

$$\frac{V_{out}}{V_{in}} < 1 \qquad \text{Eq.(2.3.38)}$$

To make sure the stability of the circuit, the calculation process is verified below:

$$\frac{V_{out}}{r_{o3}} + g_{m3}V_{gs3} + \frac{V_{out}}{R_2} = 0 \qquad \text{Eq.(2.3.39)}$$

Since from previous calculation, find that $V_{out} = V_x$

$$\frac{V_{gs3}-V_Y}{r_{o7}}+g_{m7}(V_{in}-V_Y)=\frac{V_Y}{r_{o2}} \qquad \text{Eq.(2.3.40)}$$

From Eq.(2.3.40)

$$V_Y=\frac{g_{m7}V_{in}r_{o7}+V_{gs3}}{g_{m7}r_{o7}R_2+R_2+r_{o7}}\approx\frac{g_{m7}V_{in}r_{o7}+V_{gs3}}{g_{m7}r_{o7}R_2}=\frac{V_{gs3}}{g_{m7}r_{o7}}+V_{in} \qquad \text{Eq.(2.3.41)}$$

Thus

$$\frac{V_{out}}{V_{in}}=\frac{r_{o3}}{r_{o3}+R_2}<1 \qquad \text{Eq.(2.3.42)}$$

Obviously, the gain is smaller than 1, it is stable.

However, it needs a start-up circuit to turn on the bandgap to work in the beginning. The author adds up a start-up as well as the biasing below:

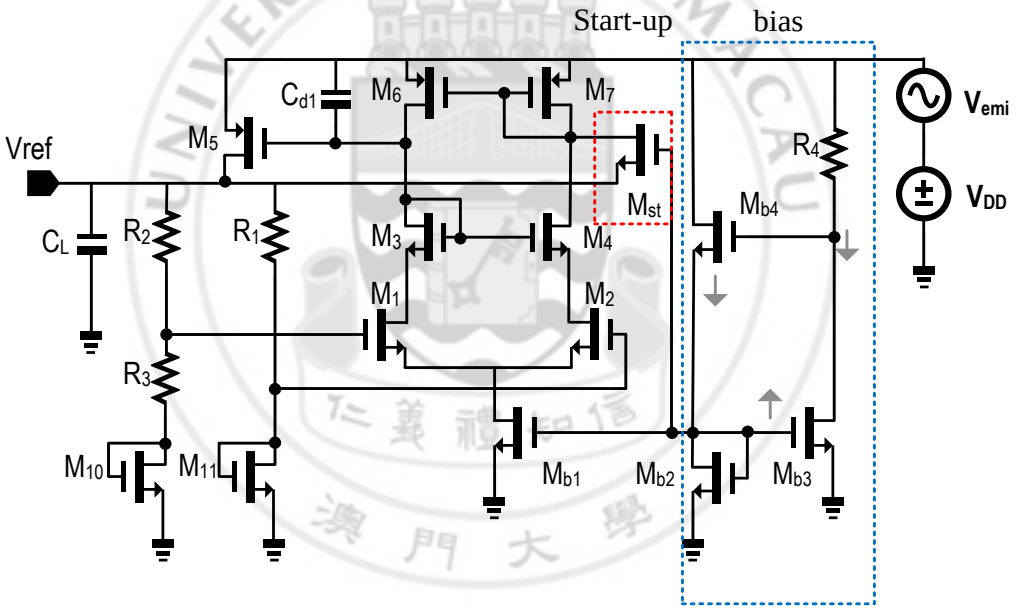

Figure 2.3.9 The bias and start-up whole circuit

For start-up circuit, when the current pass through the Mb bias circuit, the gate voltage of Mst will increase up to turn on Mst while current will pass through thus the gate voltage of M3 and M4 will turn down to decrease thus the gate voltage of M5 will increase to turn M5 on. Therefore the reference voltage will increase until it is higher to turn the Mst off. Mst has no longer use anymore.

For bias circuit, Mb2, Mb3 and Mb4 consist of a negative feedback to make the sure the tail current is kept constant, the negative feedback is shown on the circuit diagram.

The PSRR simulation result from reference node to EMI source is shown below:

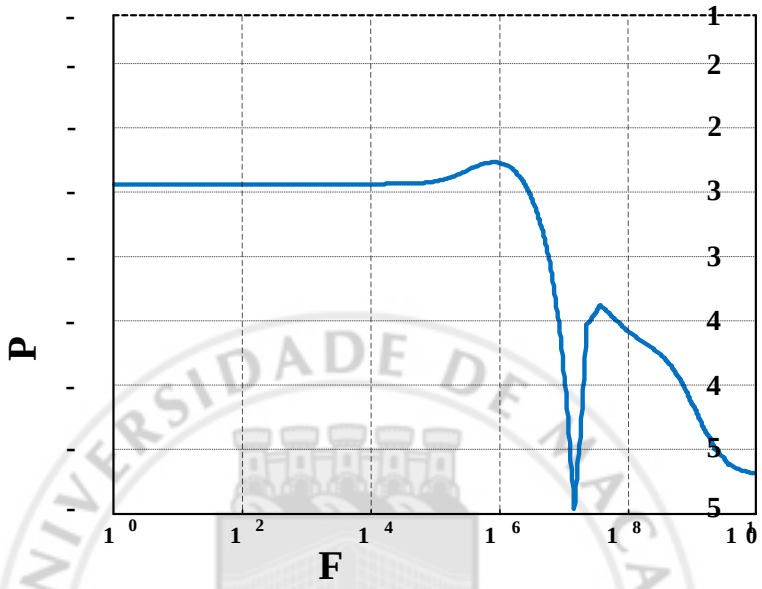

Figure 2.3.10 The PSRR simulation result from 1Hz to 10GHz

The following figures show the reference voltage and its temperature coefficient:

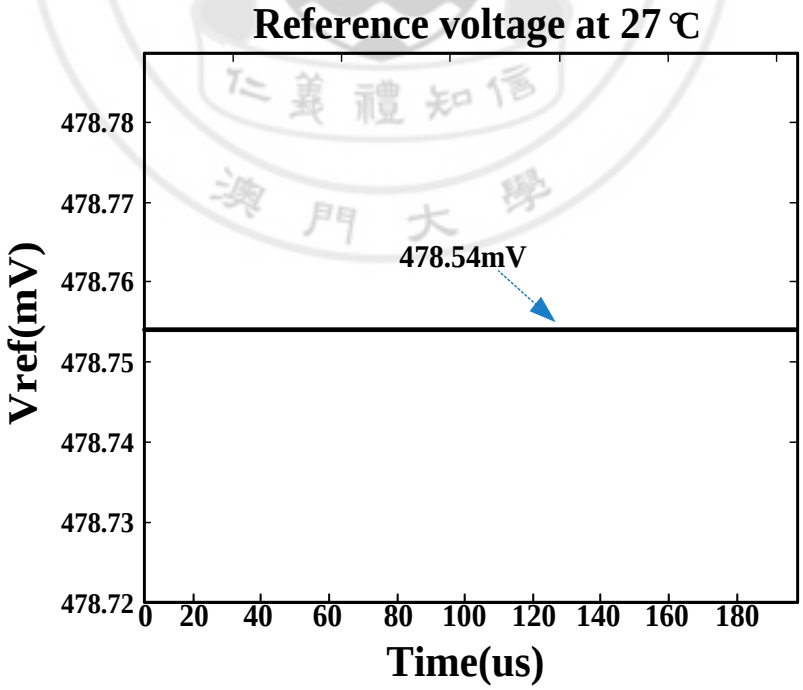

Figure 2.3.11 The reference output voltage at 27℃

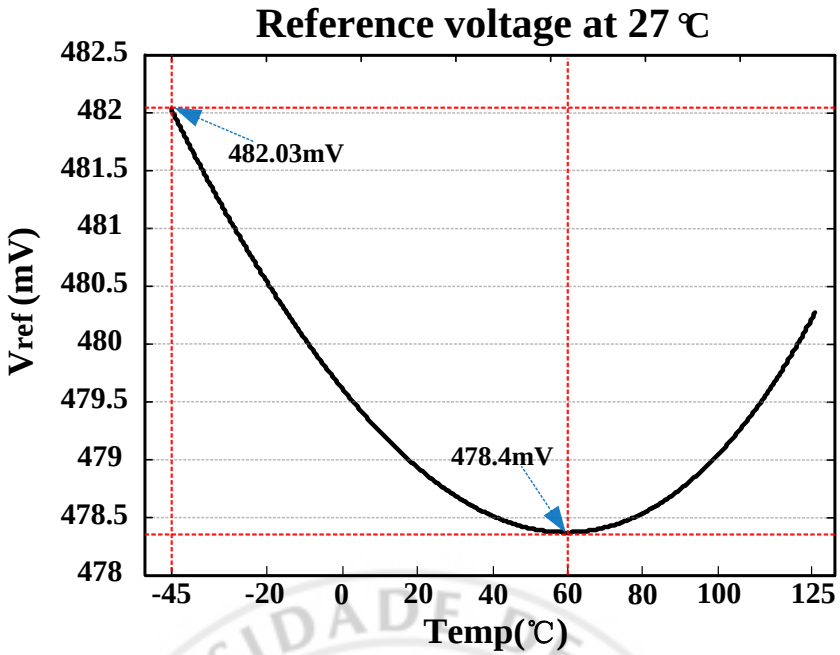

Figure 2.3.12 Reference voltage change from -45℃ to 125℃

The temperature coefficient is shown below:

$$T = \frac{V_{max}-V_{min}}{V_{ref}\times\left(T_{max-T_{min}}\right)} = \frac{482.03mV-478.4mV}{478.54mV\times(125+45)} \approx 44.62(ppm/\ ^{o}C) \qquad \text{Eq.(2.3.43)}$$

At last, the total power consummation is

$$P = UI = 1.2V \times 271.7u = 326\mu W \qquad \text{Eq.(2.3.44)}$$

2.3.2 Large signal analysis

Compare it to PPD, it has an additional improvement to solve the problem which NPD and PPD remains unsolved that the drain voltage disturbance for M1 and M2.

It adds one more current mirror M6-M7 above at the drain of input pair M1-M2. This current mirror with active load it can mask the nonlinear output resistances of M1-M2 by using positive feedback. This is illustrated in small signal analysis. The advantages are illustrated below:

1. The output impedance of the OTA is equal to r_{o3} which is independent of M1 and M2. While the original output impedance is $r_{o1} \| r_{o3}$. The out impedance also increases.
2. The drain voltages of input pair M1-M2 are kept at an equal value since they are masked by M6-M7. Less DC shift will occur.

3. M6-M7 forms a current mirror which can force the drain current I_{d1} and I_{d2} equal to each other. This will also reduce the DC shift and maintain the current distribution for the two paths.

2.3.3 Compare with PPD and PPDAL

According to the analysis, the small signal transfer equations(open loop transfer function) from power supply to reference voltage are represented schematically in Fig 3.4.1.[7]

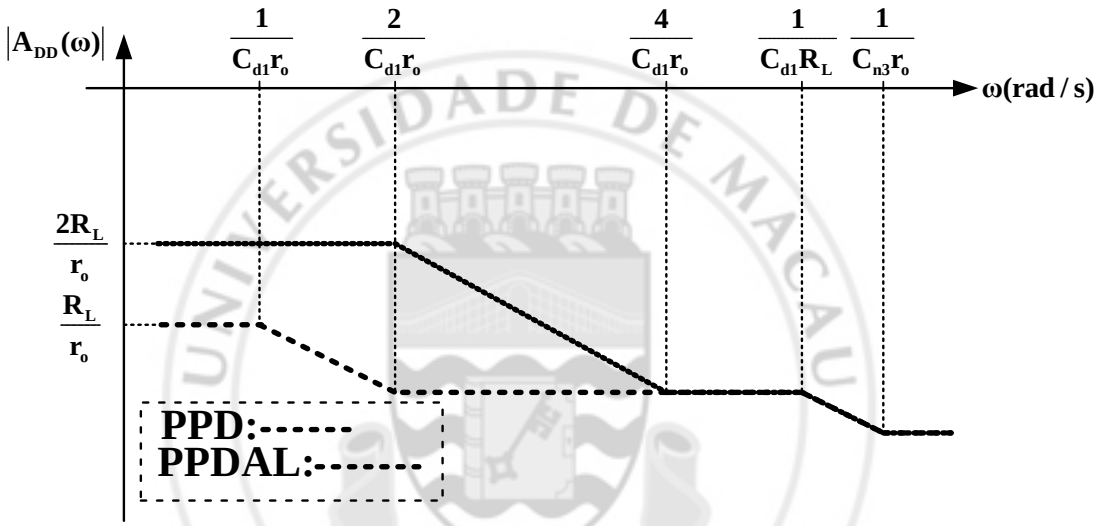

Figure 2.4.1 The comparison of open loop bode plot for PPD and PPDAL

From this schematic, it is clear to show that which parameter determines the different frequency ranges. Poles and zeros can be cancelled with each other through proper adjustment.

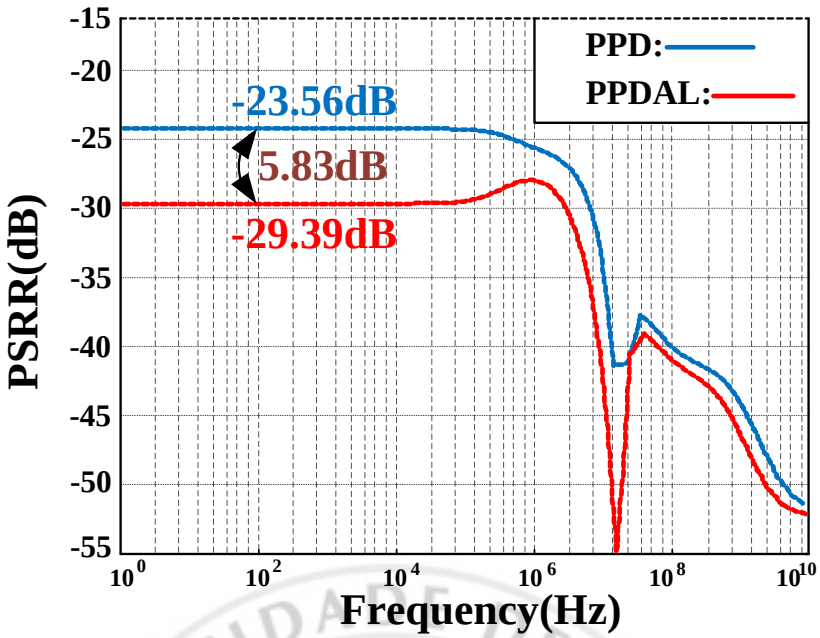

Figure 2.4.2 The comparison of PSRR for PPD and PPDAL

For PSRR, comparing it with bode plot diagram, the difference is due to that the simulation results represent the closed loop transfer function and it should include the input pair. The whole tendency of PPD and PPDAL are similar. PPD has a 5.83dB small than PPDAL in low frequency range. This is verified with the math calculation:

$$20\log\frac{2R_L}{r_o}=20\log\frac{R_L}{r_o}+20\log 2 \qquad \text{Eq.(3.4.1)}$$

$$PPD_{PSRR}=PPDAL_{PSRR}+6dB \qquad \text{Eq.(3.4.2)}$$

5.83dB is approximately equal to $20\log 2$ in simulation, is the PSRR difference of PPD and PPDAL in low frequency DC range.

In high frequency range, after the dominant poles and zeros, PPD and PPDAL have the same PSRR. They both have the same the second dominant pole. After the second pole they will decrease simultaneously.

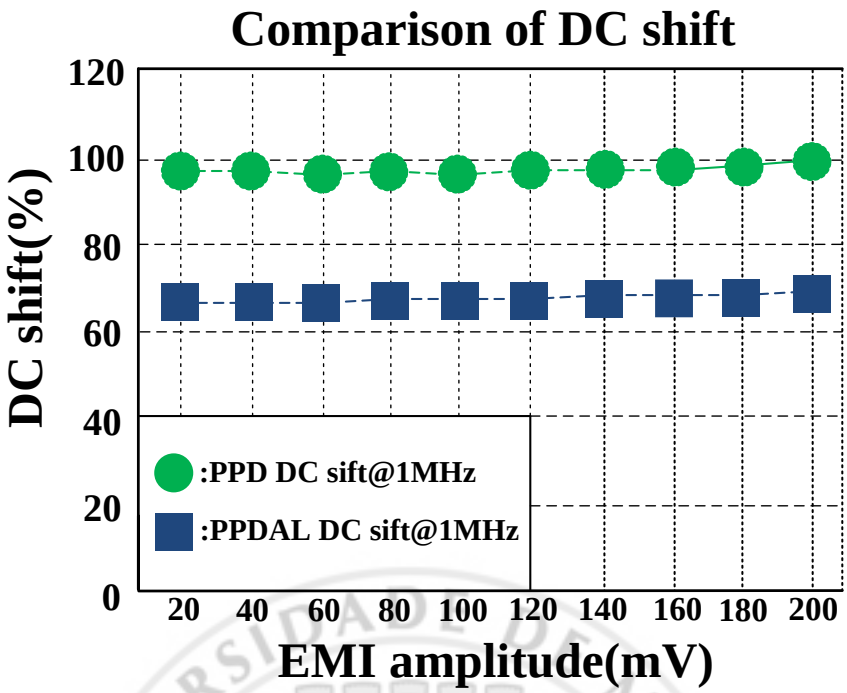

Figure 2.4.3 The comparison of PPD and PPDAL with different EMI amplitudes with same frequency

For DC shift, both of them have a larger DC shift as frequency and EMI amplitude become higher. The ability to resist EMI for PPDAL has an about 31% increase from 96.4% to 66.5% compare to PPD with different EMI amplitude at the same frequency. This is due to the adding active current mirror has masked the input pair to stable current and to have less DC shift at the drain nodes of them thus the output resistance of the OTA is independent of the input pair. The fixed value at drain node is better to have the higher prevention to cause the input pair into linear region to make DC shift.

3. Proposed PPDAL BGP

3.1The double differential input pair PPDAL

In order to increase the ability of the BGP to prevent EMI interference, F.Fiori presents a double differential input stage robust to EMI. The output offset voltage against the EMI has reduced a lot. [8] The high pass filter can guarantee the loop gain to force the two input node have equal voltages. The high pass frequency is set at 150 kHz, since the EMI full range is normally from 150 kHz to 1 GHz, as specified in the DPI specification. On the basis of PPDAL, bias circuit is also changed. The improved PPDAL circuit diagram is shown below:

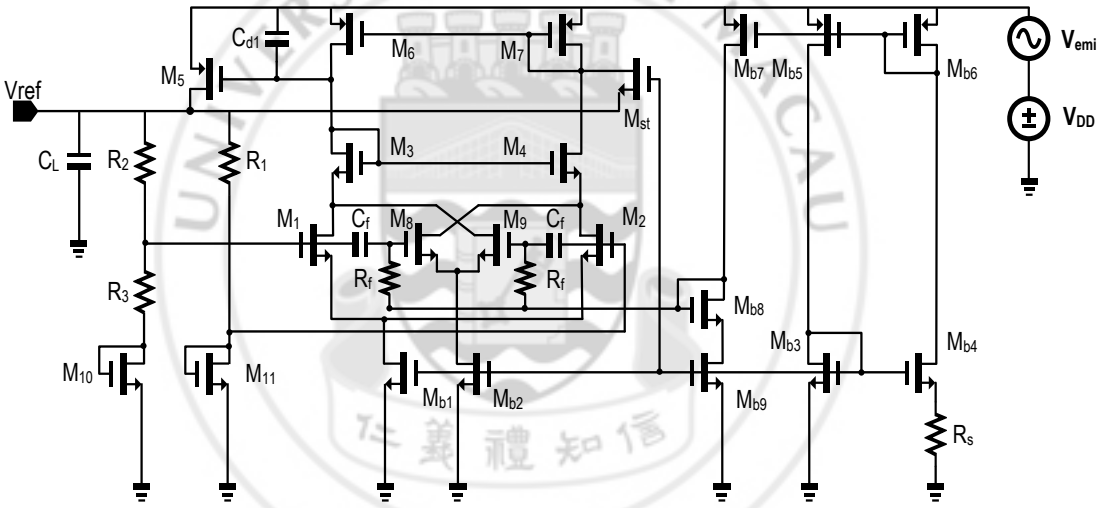

Figure 3.1 The improved PPDAL kuijk bandgap circuit

3.1.1 Small signal analysis

Illustration for each aspect one by one is shown below; when the frequency is lower than 150 kHz, the model is same as the PPDAL, the double differential pair does no work. When the frequency is higher than 150 kHz, the signal goes pass through it and its corresponding model is shown below. First to see how the double differential input stage affects the OTA gain:

The following equations will calculate the OTA gain:

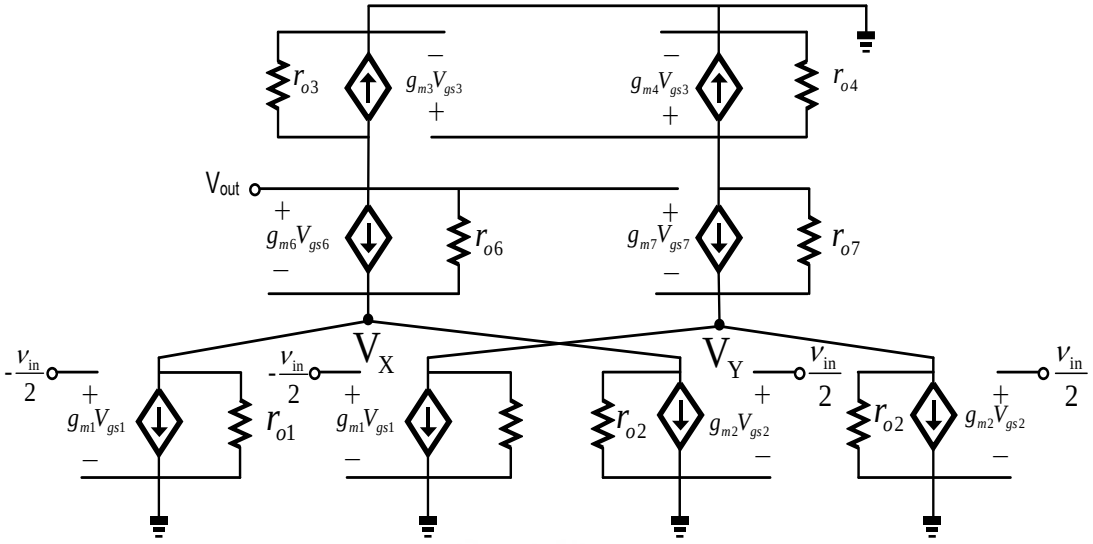

Figure 3.2 The improved PPDAL kuijk bandgap small signal circuit

$$\frac{V_{out}}{r_{o3}}+g_{m3}V_{gs3}+\frac{V_{out}-V_x}{r_{o6}}+g_{m6}(V_{out}-V_x)=0 \qquad \text{Eq.(3.1.1)}$$

$$\frac{V_{out}-V_x}{r_{o6}}+g_{m6}(V_{out}-V_x)=\frac{V_x}{r_{o1}}+\frac{V_x}{r_{o9}}+g_{m1}(-\frac{V_{in}}{2})+g_{m9}(\frac{V_{in}}{2}) \qquad \text{Eq.(3.1.2)}$$

$$\frac{V_{gs3}}{r_{o4}}+g_{m4}V_{gs4}+\frac{V_{gs3}-V_Y}{r_{o7}}+g_{m7}(V_{out}-V_Y)=0 \qquad \text{Eq.(3.1.3)}$$

$$\frac{V_{gs3}-V_Y}{r_{o7}}+g_{m7}(V_{out}-V_Y)=\frac{V_Y}{r_{o2}}+g_{m2}(\frac{V_{in}}{2})+\frac{V_Y}{r_{o8}}+g_{m8}(\frac{V_{in}}{2}) \qquad \text{Eq.(3.1.4)}$$

From Eq.(3.1.2) and Eq.(3.1.4),

$$V_X \approx V_{out}+\frac{V_{out}}{g_{m6}r_{o6}}+\frac{V_{in}(g_{m1}-g_{m9})}{2g_{m6}} \qquad \text{Eq.(3.1.5)}$$

$$V_Y \approx V_{out}+\frac{V_{gs3}}{g_{m7}r_{o7}}+\frac{V_{in}(g_{m8}-g_{m2})}{2g_{m7}} \qquad \text{Eq.(3.1.6)}$$

Substitute both of them to Eq.(3.1.1) and Eq.(3.1.3)

$$V_{gs3}=\frac{V_{in}(g_{m2}-g_{m8})}{g_{m7}(1+g_{m4}r_{o4})}+\frac{V_{in}(g_{m8}-g_{m2})r_{o4}}{2(1+g_{m4}r_{o4})}-\frac{2V_{out}}{1+g_{m4}r_{o4}} \qquad \text{Eq.(3.1.7)}$$

$$\frac{V_{in}(g_{m2}-g_{m8})}{1+g_{m4}r_{o4}}+\frac{V_{in}(g_{m8}-g_{m2})}{2}-\frac{V_{out}}{r_{o3}}+\frac{2V_{out}}{r_{o1}}+\frac{2V_{out}}{g_{m6}r_{o6}r_{o7}}+\frac{V_{in}(g_{m1}-g_{m9})}{g_{m6}r_{o6}}+\frac{V_{in}(g_{m9}-g_{m1})}{2}=0$$

Eq.(3.1.8)

Finally, the OTA gain is got below：

$$\frac{V_{out}}{V_{in}} \approx \frac{(g_{m1}+g_{m2}-g_{m8}-g_{m9})r_{o3}}{2} \qquad \text{Eq.(3.1.9)}$$

According to this result, the OTA gain is almost equal to zero if $g_{m1}+g_{m2}=g_{m8}+g_{m9}$. This is easy to satisfy, neglecting the mismatch. This is the reason why the high pass filter can't be neglected. The OTA gain is zero to cause the loop gain zero. Compare to the original PPDAL structure, the original OTA gain is $g_{m3}r_{o3}$. The new structure OTA gain is nearly 0. Which means that if there is interference at the input, it will be eliminated at the output, while not be amplified to cause disturbance. Thus, adding the cross differential pair at the input, it will do a great job to prevent to amplify the interference at the input to cause disturbance at the gate of M5. This node will only affected by the power supply which will be verified in the following part.

For DC shift, another advantage of the cross differential pair is that it can help to stable the drain voltages of the input pair better. No matter how the input changes, the drain current will try to be as stable as possible. If it has a differential interference at input, the current effect will be cancelled since one will increase and another will decrease the same amount. If it has a common mode difference at input, the current change at two nodes will be the same and it will be restricted by the tail current, so the two nodes drain voltage will be the same and stable.

For attenuating EMI, to calculate whether the PSRR of this improved one is changed or not:

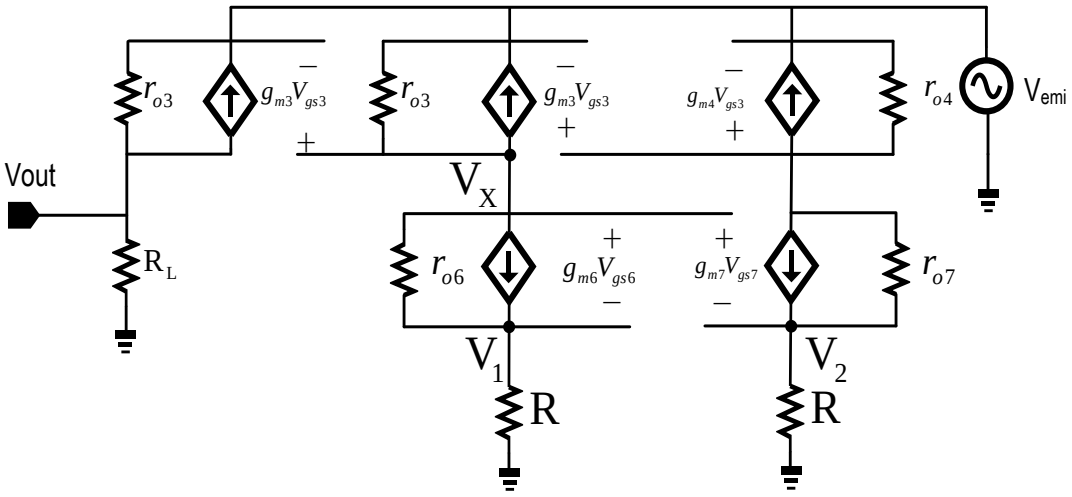

Figure 3.1.2 The improved PPDAL kuijk bandgap small signal circuit

Using KCL:

$$\frac{V_{g3}-V_{in}}{r_{o4}}+g_{m3}(V_{g3}-V_{in})+\frac{V_{g3}-V_2}{r_{o7}}+g_{m7}(V_X-V_2)=0 \qquad \text{Eq.(3.1.10)}$$

$$\frac{V_{g3}-V_2}{r_{o7}}+g_{m7}(V_X-V_2)=\frac{V_2}{R} \qquad \text{Eq.(3.1.11)}$$

$$\frac{V_x-V_{in}}{r_{o3}}+g_{m3}(V_{g3}-V_{in})+\frac{V_x-V_1}{r_{o6}}+g_{m6}(V_X-V_1)=0 \qquad \text{Eq.(3.1.12)}$$

$$\frac{V_x-V_1}{r_{o6}}+g_{m6}(V_X-V_1)=\frac{V_1}{R} \qquad \text{Eq.(3.1.13)}$$

$$\frac{V_{out}}{R_L}+\frac{V_{out}-V_{in}}{r_{o5}}+g_{m5}(V_X-V_{in})=0 \qquad \text{Eq.(3.1.14)}$$

From Eq.(3.1.11) and Eq.(3.1.13) can get that

$$V_2=\frac{V_{g3}+g_{m7}r_{o7}V_x}{1+g_{m7}r_{o7}+\frac{r_{o7}}{R}} \qquad \text{Eq.(3.1.15)}$$

$$V_1=\frac{V_X+g_{m6}r_{o6}V_x}{1+g_{m6}r_{o6}+\frac{r_{o6}}{R}} \qquad \text{Eq.(3.1.16)}$$

Substitute both of them to Eq.(3.1.10) and Eq.(3.1.12)

$$V_{g3} \approx V_{in} - \frac{V_X}{g_{m3}R} \qquad \text{Eq.(3.1.17)}$$

$$-\frac{V_X}{R} + \frac{V_X - V_{in}}{r_{o3}} + \frac{V_X(1+g_{m6}r_{o6})}{R+g_{m6}r_{o6}R+r_{o7}} = 0 \qquad \text{Eq.(3.1.18)}$$

$$V_X \approx V_{in} \qquad \text{Eq.(3.1.19)}$$

Till now, the output node of the OTA is almost equal to Vin, the same as before.

$$\frac{V_{out}}{V_{in}} \approx \frac{R_L}{r_{o5}+R_L} \approx \frac{R_L}{r_{o5}} \qquad \text{Eq.(3.1.20)}$$

R is equal to the paralleling of two input resistors which is almost equal to half of their resistance value since both of them have the same size. Finally the PSRR gain of the new structure from source to output is the same to the PPDAL structure. It is unrelated to the input pair. It is dependent on the output loading resistor and the PMOS drain source resistor. So the new structure will not attenuate the PSRR.

Since why this bandgap has a lower PSRR, this is due to the output loading resistor has increased in order to have a better temperature coefficient, this will be discussed later.

For the bias problem, in this bandgap, the power supply independent bias structure is chosen to bias the tail current:

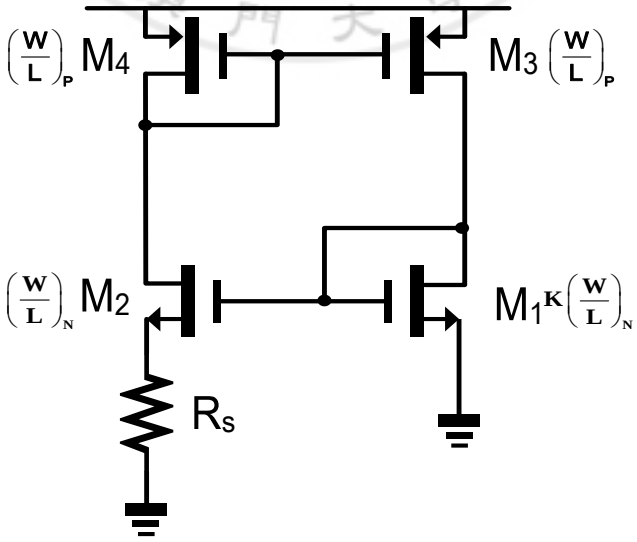

Figure 3.1.3 The power supply-independent bias circuit

Comparing to the PPDAL bias, it can adjust the current to bias which means it can reduce the bias current to save power consumption. If use the PPDAL bias, since it needs to adjust the MOSFETs into strong inversion region thus the voltage drop across the resistor is large, to have small current, it needs a quite large resistance value to realize, it will take more space and induce larger thermal noise.

Another advantage is that the bias current is independent of power supply which shows that within the transistor's voltage swing enduring ability, the bias current is resisting to the electromagnetic interference in the power supply. The following equations will verify it:

$$\sqrt{\frac{2I_{out}}{\mu C_{ox}(W/L)_N}}+V_{TH1}=\sqrt{\frac{2I_{out}}{\mu C_{ox}K(W/L)_N}}+V_{TH2}+I_{out}R_S \qquad \text{Eq.(3.1.21)}$$

$$\sqrt{\frac{2I_{out}}{\mu C_{ox}(W/L)_N}}(1-\frac{1}{\sqrt{K}})=I_{out}R_S \qquad \text{Eq.(3.1.22)}$$

$$I_{out}=\frac{2}{\mu C_{ox}(W/L)_N}\frac{1}{R_S^2}(1-\frac{1}{\sqrt{K}})^2 \qquad \text{Eq.(3.1.23)}$$

Assume that V_{TH1} and V_{TH2} are almost equal to each other. Thus can get that the current is only related to the size and the resistor value, which is independent of power supply if don't conclude the process and temperature variation.

However, there is also one problem which needs to keep in mind is the precondition to get final equation is that I_{out} can't be zero. In this case, to ensure $I_{out} \neq 0$, adding an start-up to avoid this case.[9]

The simulation results are shown below:

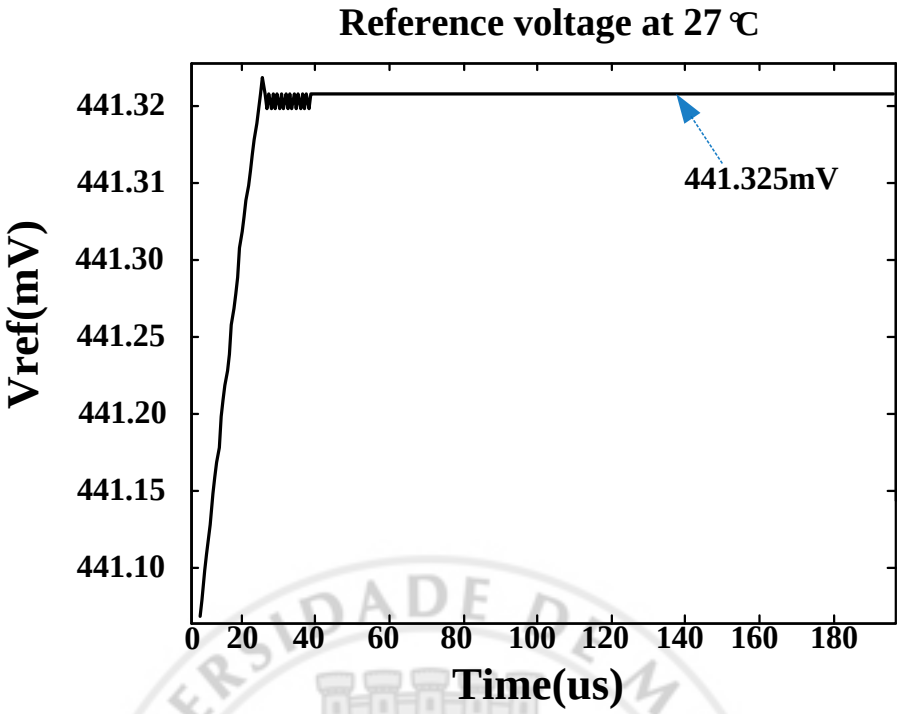

Figure 3.1.4 The reference output voltage at 27℃

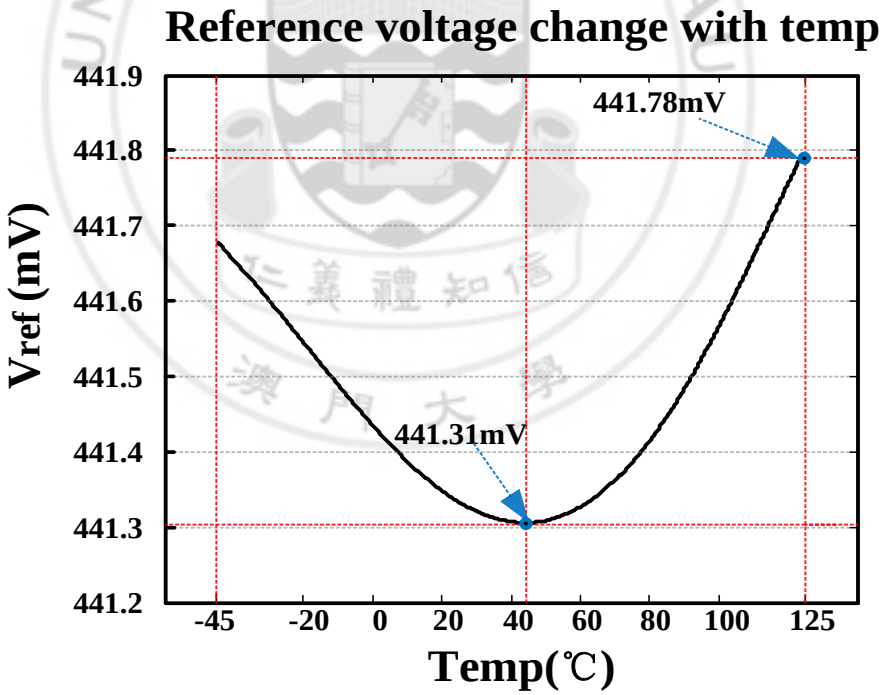

Figure 3.1.5 Reference voltage change from -45℃ to 125℃

The maximum voltage is 461.78mV and the minimum voltage is 441.325mV. The temperature coefficient (TC) has improved from 44.62(ppm/℃) to 10.65(ppm/℃). The voltage variation with temperature change has improved a lot.

$$T = \frac{V_{max}-V_{min}}{V_{ref}\times\left(T_{max-T_{min}}\right)} = \frac{441.78mV-441.31mV}{441.325mV\times(125+45)} \approx 10.65(ppm/\ ^{o}C) \qquad \text{Eq.(3.1.24)}$$

This is the PSRR simulation result:

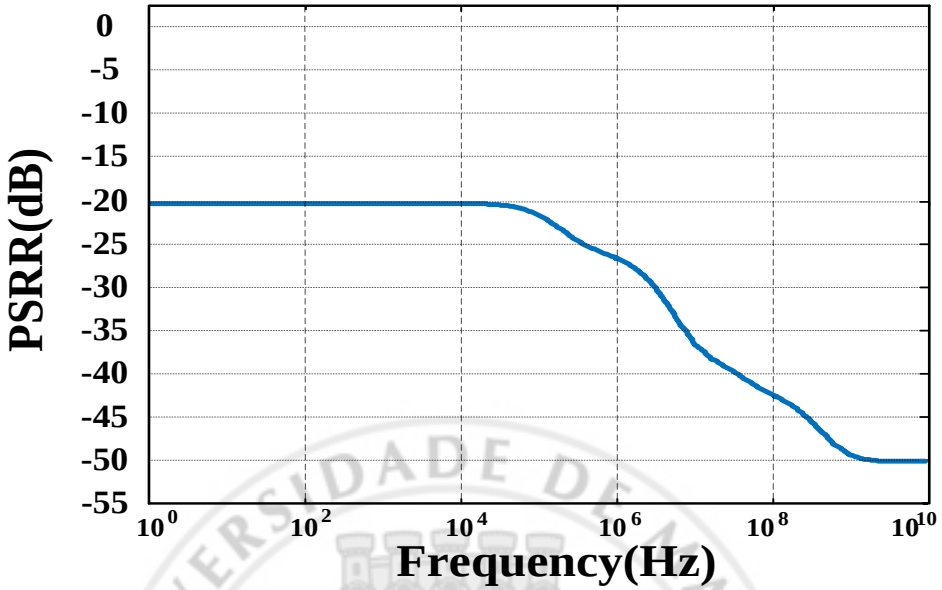

Figure 3.1.6 The PSRR simulation result from 1Hz to 10GHz

The following shows the EMI sustain ability and its DC shift of the improved PPDAL BGP:

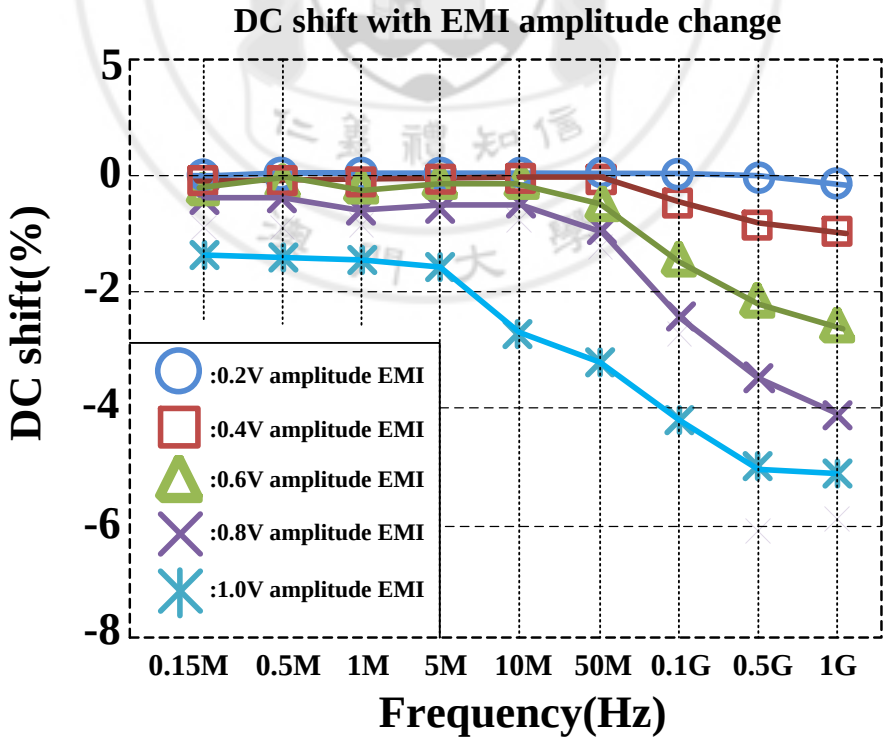

Figure 3.1.7 The DC shift with different EMI amplitudes change

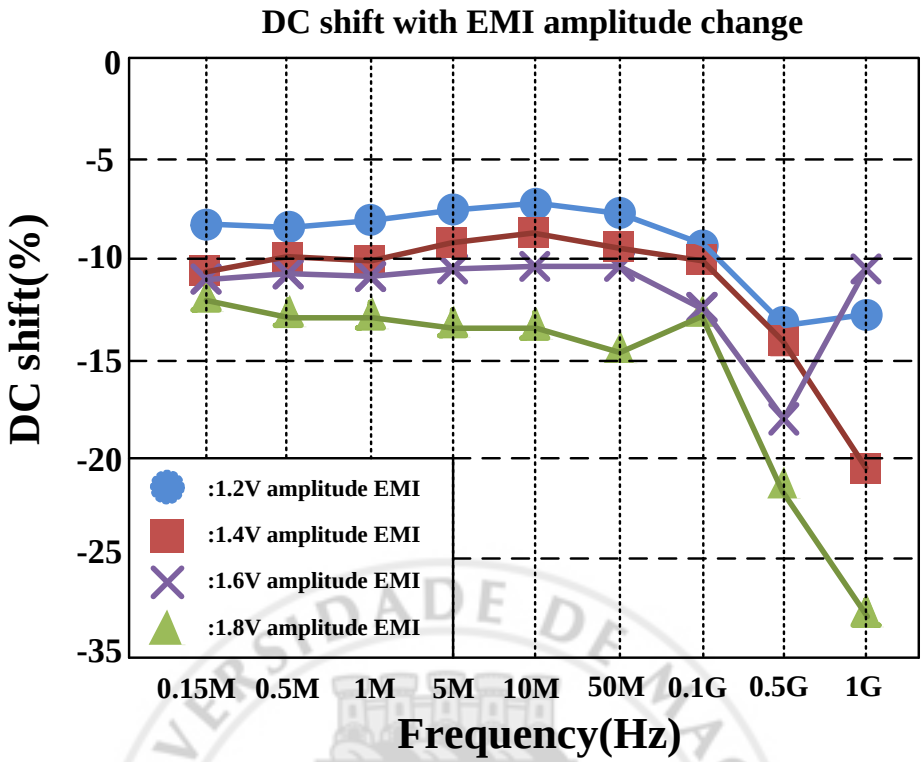

Figure 3.1.8 The DC shift with different EMI amplitudes change

From above two figures for the improved PPDAL bandgap, the DC shift is rising with the larger value EMI signal as well as with higher frequency. The tendency is also the same. Under 1.2V amplitude EMI, the DC shift is smaller than 3% below around 100MHz. For beyond 1.2V amplitude EMI, the DC shift is relatively around 10% below around 100MHz; and with frequency larger 100MHz, the change of DC shift is larger comparing to low frequency range. For larger EMI amplitude, even though the DC shift has prevented a lot, the large swing will also cause the MOSFET clipping or rectification to make DC shift. For higher frequencies, this is due to some of the parasitic capacitances in the circuit to change the value of the signal and affect the DC shift. Generally, the DC shift change is within what expected and not have large fluctuations.

3.1.2 Large signal analysis

Since that the origin of DC shift lies in the accumulation of an asymmetric nonlinearly distorted signal, for high EMI amplitude signals, Strong nonlinear

behavior is the nonlinearity which is generated when active devices are brutally switched on and off, rectification will be shown. It is in general not possible to obtain accurate closed form expressions of circuits behaving in a strong nonlinear way [10], since it needs to conclude more terms into consideration. It will affect the work condition of the circuit. The voltage will be clipped or distorted depends on how large the interferences will affect the component.

This DC shift increases the average output current, and consequently decreases the mean output voltage. The DC shift on the output equivalently converges towards a value which is characterized by the DC value of the gate source voltages.

The following equations will illustrate the DC shift：

$$I_{d\_with}EMI = \lim_{T\to\infty}\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} I_{d1}(t)dt = \overline{\frac{1}{2}\mu Cox\frac{W}{L}(V_{SG5}+v_{sg5}-|V_{TH}|)^2}$$

Eq.(3.1.25)

$$=\overline{\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{SG5}-|V_{TH}|)^2}+\overline{\mu C_{ox}\frac{W}{L}(V_{SG5}-|V_{TH}|)v_{sg5}(t)}+\overline{\frac{1}{2}\mu C_{ox}\frac{W}{L}v_{sg5}^2(t)}$$

Eq.(3.1.26)

So for any one period, the first term is the wanted DC term, it is the desired DC bias current. The second term is within the EMI signal and it is linear proportional to the EMI signal with time, its average value is zero. The third term is proportional to the square of the EMI signal, its average value will not be equal to zero, and so this term is responsible for DC shift.[1]

However, this is only correct when EMI signal is not large enough. For large amplitude EMI, The equation is no longer suitable, since distortion may occur, the transistors may brutally switched on and off, clipping will appear. For high frequency EMI signal, it will induce harmonic interference to cause DC shift. This is the first issue needs to be concerned.

The large EMI for positive and negative swings, this has been told in NPD. For positive EMI swing, the large signal output resistance for M1 and M2 will decrease due to velocity saturation. For negative EMI swing, the input pair M1 and M2 will be

forced into linear region and thus the output resistance will increase. Owing to different drain voltages, it will produce different average drain current. The current sum will be restricted by the tail current. Therefore, to fix the drain voltage stable and equal to each other is predominant. The double differential pair can basically solve this problem to cancel the current increase and decrease at the drain voltage node.

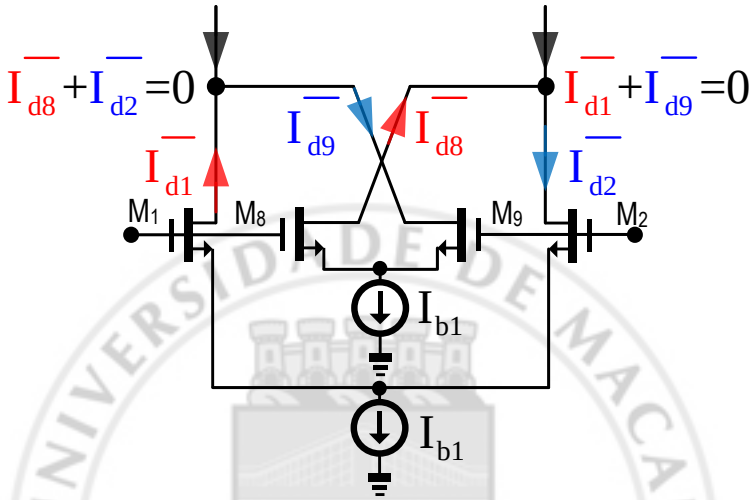

Figure 3.1.9 The double differential pair current change when EMI injection

From above figure, it is clearly to see the average drain current shift at the drain node is equal to zero. The double differential input pair cancels each other to make a balance to stable the current.

3.2 Comparison

The comparison with PPDAL and how it improves:

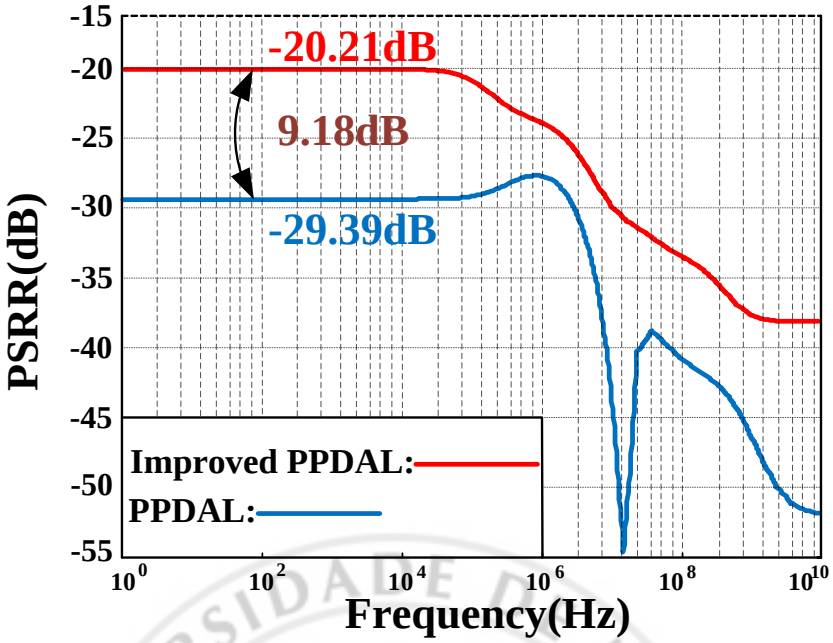

Figure 3.2.1 The comparison of PSRR for PPDAL and the improved one

Even though the improved PPDAL and the PPDAL have the same PSRR equation, the difference is due to the unequal value of the resistances for improving the temperature coefficient. Due to the differences between 10^6 Hz and 10^8 Hz，the BJT has changed to MOSFET, thus it induces the parasitic capacitances to produce poles and zeros at the gate of input pair. It needs to be carefully adjusted to cancel the poles and zeros to let the PSRR curve smoothly goes down, just as the equations and bode plot as BJT does.

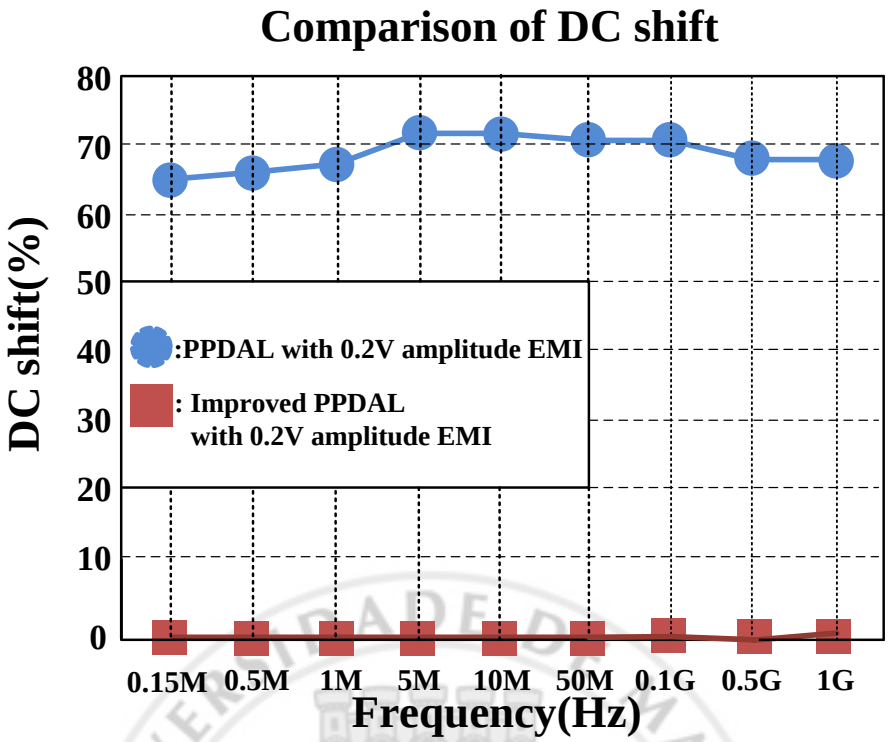

Figure 3.2.2 The Comparison of DC shift with same 0.2V EMI amplitude

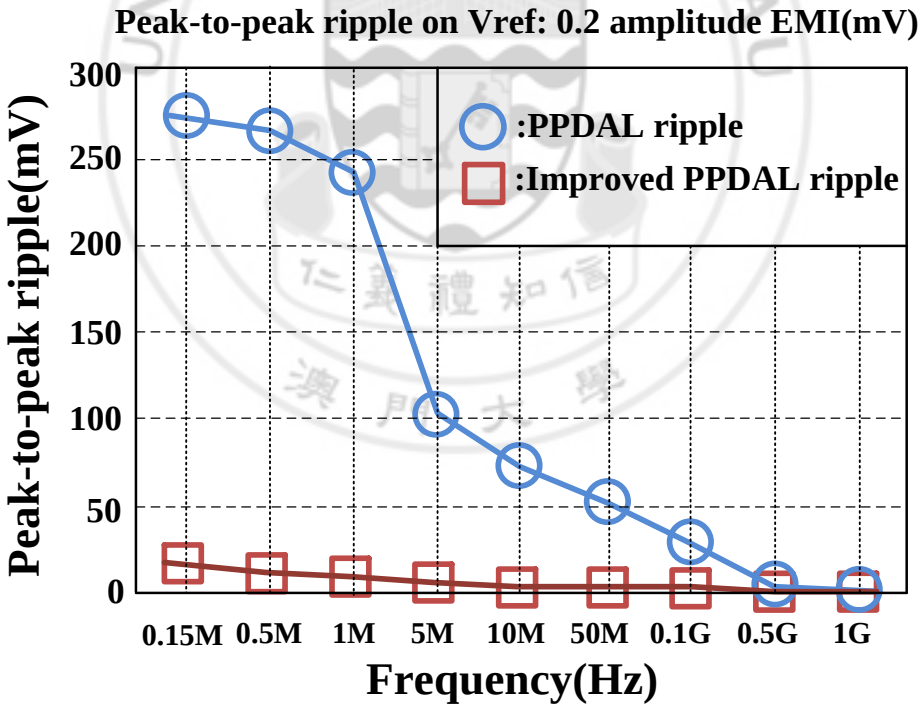

Figure 3.2.3 The Comparison of Peak-to-peak ripples with same 0.2V EMI amplitude

Compare with PPDAL, with the same EMI signal, the DC shift has improved a lot, it improves from around 65% to 0.1%. To PPDAL, in the relatively low frequency range, the peak to peak ripple is quite large. It doesn't match to the corresponding PSRR value. I think the OTA seems doesn't work due to the unstable tail current; the power supply is only 1.2V, some voltage variations will cause the circuit out of work since the voltage headroom is quite small. As frequency becomes higher, the peak to peak ripple has decreased fit with PSRR, the signal couples through capacitor to let the M5 work. It is quite unstable with different frequencies and different EMI.

For this improved PPDAL bandgap, the adding differential cross couple can prevent the DC shift at the drain nodes of the input pair better and also the tail current is biased without the power supply voltage variations which can be fixed stably. Thus within a valid EMI sustain range, the DC shift is nearly equal to 0, and the peak-to-peak ripple is related by the PSRR, thus to have a better rejection, increasing PSRR is crucial. The peak to peak ripples also reflect the corresponding PSRR value not have the distortion which means the circuit works normally. Since the reference voltage isn't high enough, the voltage load the MOSFET can sustain and the power supply voltage. It determines that the maximum EMI signal resisting level is limited.

The power consumption is constituted by three parts: the bias, the OTA and the output loading. For the improved PPDAL, it is mainly reduced from the bias from 198.72**μ**A to 14.06**μ**A. It can produce the same amount of current with smaller resistance value and the bias current is adjusted freely. For loading, the power consumption is related to the temperature coefficient. With proper design it can be reduced also.

The temperature coefficient (TC) only solves the first order compensation. Since the output loading resistor R_L is related to the PSRR attenuation equation as well as

the TC. These two are the tradeoffs as well. Thus to increase the TC, PSRR will be sacrificed. Thus the proper adjustment of R_L is quite important.

4. Conclusion

In this these, the performance of the electromagnetic interference resisting circuit is a low reference voltage(441.3mV) bandgap which is improved by achieving 10.65ppm/ ^{o}C TC, 104μW and can work against 2V amplitude EMI.

Table:

The work performance comparison

		PPDAL	This work
TC(ppm/℃)		**44.62**	**10.65**
Power(μW)		**326**	**104**
Max EMI resisting amplitude(V)		**0.2**	**2**
DC shift @ 0.2V EMI Amplitude(%)		**66.5**	**0.1**
PSRR(dB)	**@150KHz**	**-29.24**	**-21.61**
	@1GHz	**-46.23**	**-49.53**

Table4.1 The total comparison for PPDAL and the improved one

5. Reference

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