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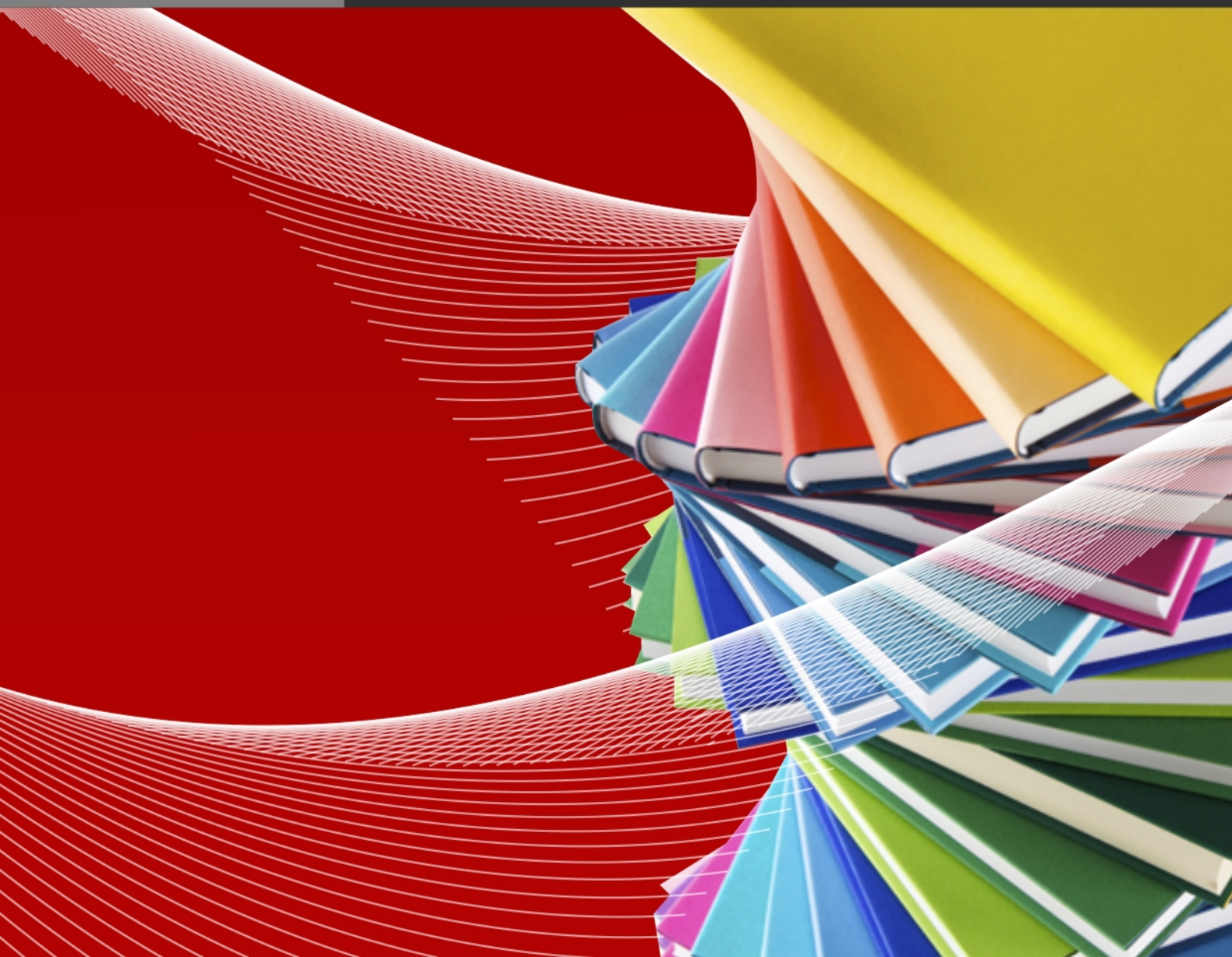

# A 107dB DR, 106dB SNDR Sigma-Delta ADC Using a Charge-Pump Integrator for Audio Application

By

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# ABSTRACT

Real world are full of analog signals, such as sound, light and color. After the electronic revolution change came in, the magic brings novel device become a sort of clear existence, like film, mobile, radio. Sure, we can imagine the first people hearing the unclear voice from the telephone, the digital world is still a bounded existence with noise and distortion. But as a development, people are expecting for clear information and instructions, which means an extensive bridge between the analog and the digital world.

To reach the goal, a high performance system which is called analog-to-digital converter (ADC) is necessary. It is worked in electronic circuits at the interface between the analog and the digital world. In this Final-Year-Project, we focus on the digital audio conversion as we are probably pretty sure of being told that we're in the middle of a digital audio revolution. In fact, for a hi-tech musician with an interest in computing and digital audio hardware, chances are more aware of the possibilities than most people.

Comparing to other application like wireless communication, audio application covers a relatively narrow bandwidth but needs high resolution, due to that, Sigma-Delta ($\Sigma-\Delta$) modulation based analog-to-digital (A/D) conversion technology is used in our system design as a cost effective alternative for high resolution (greater than 12 bits) converters which can be ultimately integrated on digital signal processor ICs. In this project, the Cascaded Resonator with Distributed Feed Forward (CRFB) is selected because of its high SNR and the narrow swing. Plus, a capacitive charge-pump is used to improve the power efficiency of the first stage amplifier. By using 3rd order CRFB architecture with charge-pump in the first stage, the simulated FOM is 204fJ/conversion-step from 1-V supply. This CP based modulator gives 106dB peak-SNDR and 107dB dynamic range over a 20 kHz bandwidth with 1.332mW power consumption, almost 32 % lower than that of the convention one.

# ACKNOWLEDGMENT

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It is an honor for us that is given the opportunity to develop our own individuality and self-sufficiency by being allowed to work with such independence. The experience working in State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau will chase us for the future. If we have seen further it is by standing on the shoulders of Giants.

We are grateful to many colleague for the completion of this project, all these people read the evolving manuscript and circuits and offered advice. And because of their help, we are content with the final result. Among them, we are particularly grateful to Qi Liang, Wang Biao, for their reviewing the technical contexts and elaborative debugging.

Moreover, as a two people's team, it was a great comfort and relief to know that we were willing to share the working experience, we survived the experience of undergraduate school and learned to work with encouragement and patience. We gained so much a driving ability to tackle challenges. My heartfelt thanks.

Finally we would like to thank our families for their support and patience during the past semesters which has taken me to graduate.

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# List of Symbols

| SYMBOL | THE EXPLANATON |
|---|---|
| ADC | Analog-to-Digital Convertor |
| $A_0$ | Open Loop Gain |
| CIFB | Cascaded Integrators with Distributed Feedback |
| CIFF | Cascaded Integrators with Distributed Feed Forward |
| CLK | Clock Signal |
| CMFB | Common-Mode Feedback |
| CP | Charge-pump |
| CRFB | Cascaded Resonator with Distributed Feed Forward |
| CRFF | Cascaded Resonator with Distributed Feedback |
| DAC | Digital-to-Analog Convertor |
| DR | Dynamic Range |
| ENOB | Effective-Number-of-Bit |
| $f_b$ | Signal Bandwidth |
| $f_s$ | Sampling Frequency |
| FoM | Figure-of-merit |
| GBW | Gain Bandwidth |
| GND | Ground |
| NTF | Noise Transfer Function |
| OSR | Oversampling Ratio |
| PSD | Power Spectrum Density |
| SNDR | Signal-to-Noise and Distortion Ratio |
| SNR | Signal-to-Noise Ratio |
| SQNR | Signal-to-Quantization Noise Ratio |
| SR | Slew-Rate |
| STF | Signal Transfer Function |
| SW | Switch |
| THD | Total Harmonic Distortion |
| $V_b$ | Bias Voltage |
| $V_{cm\text{-}in}$ | Input Common-Mode Level |
| $V_{cm\text{-}out}$ | Output Common-Mode Level |
| $V_{DD}$ | Supply Voltage |

| | |
|---|---|
| $V_{in}$ | Input Voltage |
| $V_{out}$ | Output Voltage |
| $V_{ref}$ | Reference Voltage |
| $V^2_{n,Q}$ | Power of Quantization Noise |
| $V^2_{n,b}$ | Power of Quantization Noise within Signal Bandwidth |
| $V^2_{sin}$ | Power of Full-Scale Sine Wave |
| $\Phi$ | Phase |
| $\Delta$ | Quantization Step |
| $\varepsilon$ | Quantization Error |

# I INTRODUCTION

## 1.1 Audio Application

Real world are full of analog signals, such as sound, light and color. After the electronic revolution change came in, the magic brings novel device become a sort of clear existence. How many things could you shape out with digital clay? The answer seems to be a very large number with scientists' shading and decorating : telegram ,phone, fax, e-mail, film, digital camera, CD player, smart cards, and so on and all so rapidly, so continuously, that why it's always so exquisite and exciting to catch our breath.

During them I would like to examine audio in details. By age four, most humans have developed an ability to communicate through oral language. These unique abilities of communicating through a native language clearly separate humans from all animals. That's why voice, or audio, takes a special status in both analog and digital world.

Remember the first time you heard the music or your own voice from the speaker? Melody and rhythm can trigger feelings from sadness to serenity to joy to awe; they can bring memories from childhood vividly back to life. Maybe that's why people are favorite of music, and they are also persuading a better music device.


Figure 1 The way people listen to music [41]

So clearly one kind of important audio applications is coming from listeners, they are looking forward to better music experience. Through Figure 1, from Gramophone to CD player, new cellphone, listeners would no longer have to drive to store if they wanted the latest album – it was available at the click of a mouse and was sometimes

cheaper than a physical CD. And from our experience people are now comfortable with the idea of digital downloads and data syncing, and have grown used to surfing the internet for music whenever they are in a Wi‑Fi hot spot. For them, the first need is easier to carry as well as low power consumption.

However, professional's world is another story, from Figure 2, it shows a closed environment for recording music. Modern work flows may involve literally thousands of effects and operations. With high performance audio equipment, when we create and produce music we can use the dynamic range to aid musical expression. We can even gently plucked guitars and booming techno bass lines all in one song, or combine every sound going from a whisper to a scream. For them the first need is the audio performance.

Figure 2 Professional Audio Applications [41]

## 1.2 Analog V.S. Digital

Why the analog signal often converting into digital domain? To answer this problem, the differences between analog signal and digital signal should be known first.

From the Table 1, it shows the difference between the analog signal and digital signal. And as conclusion there are three main benefits of using digital signal instead of the analog signal,

- ✧ Increase the quality; reduce the noise and cumulative distortion. In analog transmission, it uses amplifier to amplify the attenuation signal on passage. At the

same time, the cumulative distortion increase because the noise and error come from surrounding environment also be amplified.

- ✧ Save energy, use converter instead of the amplifier in transmission.
- ✧ Information safety. We can use own method to encode and decode the signal. Given the timing information, the transmitted waveform can be reconstructed.

Therefore, the analog signal are often converting into digital domain as the higher and higher performance ADC are used in digital device nowadays.

Table 1 Difference Between Analog And Digital Signal

| | Analog | Digital |
|---|---|---|
| Signal: | Continuous signal which represents physical measurements. | Discrete time signals generated by digital modulation. |
| Waves: | Denoted by sine waves | Denoted by square waves |
| Representation: | Uses continuous range of values | Uses discrete or discontinuous values |
| Example: | Human voice in air, analog electronic devices. | Computers, CDs, DVDs, and other digital electronic devices. |

## 1.3 Background

At the beginning, knowing the characteristic of the audio is important. Sound is a mechanical wave that is an oscillation of pressure transmitted through some Medium.

- **The frequency range**

For the body, ear is a magical part because it can help humans and animals to hear the sound on around them. Sound cannot be seen, but it can be felt by vibrations. Hear sense is one of the most important senses of the body. Sound actually consist of waves and vibrations. Sound travels through the media such as air, the ground, the water, and some solid.

Frequency is the number of vibrations that are produced per second. The unit of the frequency is hertz which is described vibration per second. A low frequency sound will

have a low pitch, such as the sound when knock the door. While a high frequency sound will have a high pitch, a dolphin bark is a good example. However, humans cannot hear sounds in very high as well as very low frequency. 20 to 20,000 hertz for a healthy young person is the hearing range. [33]

- **Hearing range of humanity**

Sound pressure level (SPL) or sound level is a logarithmic measure of the effective sound pressure of a sound relative to a reference value. It is measured in decibels (dB) above a standard reference level. The standard reference sound pressure in air or other gases is 20 μPa, which is usually considered the threshold of human hearing (at 1 kHz). [16]

Then we collect data for the opposite extreme, the 'threshold of pain. This is the point where the audio amplitude is so high that the ear's physical and neural hardware is not only completely overwhelmed by the input, but experiences physical pain. Collecting this data is trickier. You don't want to permanently damage anyone's hearing in the process.

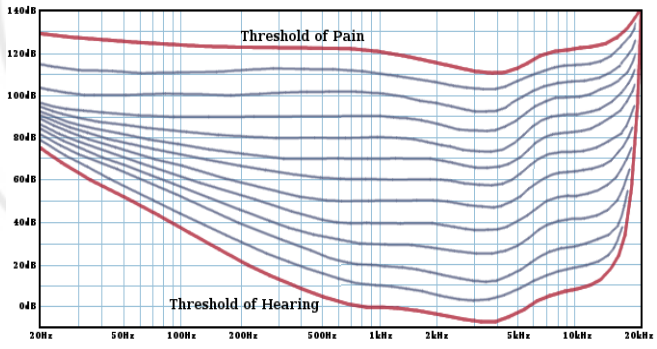



Figure 3 The threshold of pain [16]

- **CD standard**

CD is a common application of the audio. And it develops many years so there is a quite formal standard of the audio. From the CD standard, we can know about the audio standard which is used in music industry. So that it is helpful to know more about the audio. Compact Disc Digital Audio (CDDA or CD-DA) is the standard format for audio Compact Discs. The standard is defined in the Red Book. [43]

✧ 16 bit (CD standard)

Form the previous part, the sound amplitude that can be perceived by human ear is between 0 dB SPL and 130 dB SPL. Supposing the normal condition, the music that we daily heard is between 10 and 100db SPL (which is actually very high, possible screw people's ears), yields a dynamic range of 90 dB. That's why CD standard is enough for being distributed to consumers, and keeps itself for a very long time

✧ 24 bit (SACD or DSD)

But for professional, actually it's another story, Professionals use 24 bit samples in recording for headroom, noise floor, and convenience reasons like equipment matching. Also, re-production, which means mixing or mastering, needs high resolution than people's normal thinking.

DSD or SACD cancels the PCM part, it records the data at a very high rate with one-bit style. This Specifications' benefit can be well showed in the process of trying to maintain data integrity. And this is just how the high speed ADC works. This standard is advanced and well adopted by markets.

## 1.4 Types of A/D Converter

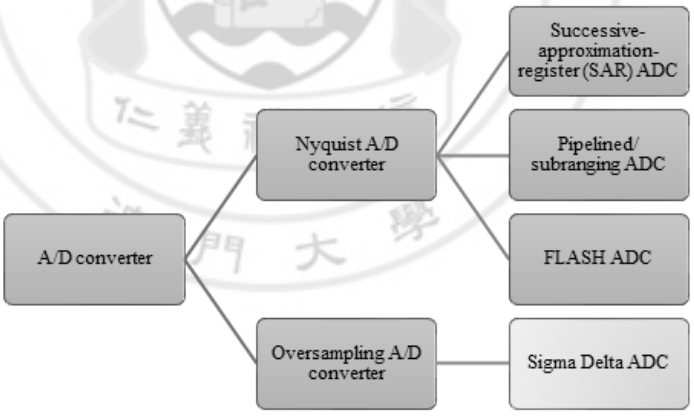



Figure 4 Different types of ADCs

It seems to be a formidable task to select the proper ADC for a particular application, considering the thousands of converters currently on the market. Going right to the selection guides and parametric search engines is a direct approach, such as those available on the Analog Devices website. Type some key words such as 'sampling rate', 'resolution', 'power supply voltage' as well as other important properties, and click the

‘find’ button to hope for the best. It’s not enough obviously. How to find a ‘best choice’ for the project as well as the application? The important approach is to get greater understanding for the task as well as the ADC.

For ADC, it can be grouped into two categories which are Nyquist ADC and Oversampling ADC according to the sampling frequency.

So, six popular ADC architectures are using to manufacture the analog-to-digital converters (ADC). To decide on the correct ADC requires tradeoffs between resolution, dynamic performance, static performance, channel count, power consumption, size, conversion time, and price. [23]

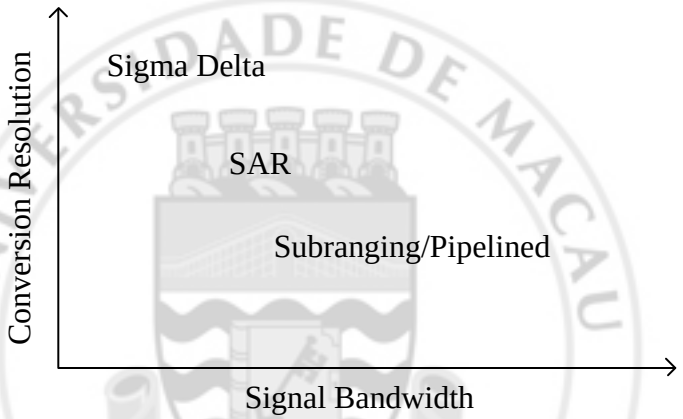



Figure 5 The operating features of Different ADCs [4]

FLASH ADC has ultra-high speed and the power consumption is not primary concern very large bandwidths.

SAR ADC has high resolution (8 to <16 bit), 5Msps and under conversion rate and low power consumption in small size.

Pipeline ADC has high speed (few Msps to 100+ Msps) and a medium to high resolution (8 to ~14bit) with lower power consumption compared with FLASH. [23]

Comparing with others, sigma-delta has high resolution (>16bit) with low bandwidth, which is suitable for the digital audio application. Therefore, sigma-delta ADC is the best choose for audio application.

- **Why sigma-delta is popular?**

For sigma-delta modulation, it has become popular modulation for high resolution application. Two significant technique of the method are oversampling and noise

shaping. Therefore the analog signals can be converted by using a 1-bit ADC only.

Though concepts of sigma-delta modulation have proposed from the Middle of the century, but this method has become more attractive only in the last two decades. The important reason is that development in VLSI technology nowadays focuses on building high speed, high intensive packed digital circuits, and it made possible the suitable digital processing into the bit stream. At low to medium signal bandwidths, it can obtain high resolution by using sigma delta modulation. [21]

All in all, sigma delta ADC is a perfect choice to the audio application.

# II BASIC THEORY OF SIGMA-DELTA ADC

## 2.1 Sampling

The digital side of a sigma-delta converter, which is what makes the sigma-delta ADC inexpensive to produce, is more complex. It performs filtering and decimation. To understand how it works, we must become familiar with the concepts of oversampling, noise shaping, digital filtering, and decimation. Especially, the oversampling and noise shaping is technique of sigma-delta ADC.

In order to learn about oversampling, it should be first know that Nyquist rate conversion, in signal processing, sampling is the reduction of a continuous signal to discrete signal.

$$X_s(f) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} X(f - kf_s) \quad (1)$$

($f$s) represents the spectrum of the sampled signal.

($f$) represents the spectrum of the original continuous time signal.

For Nyquist ADC, sampling frequency fs should be double of the bandwidth $f_B$ according to the Nyquist theory. [29]

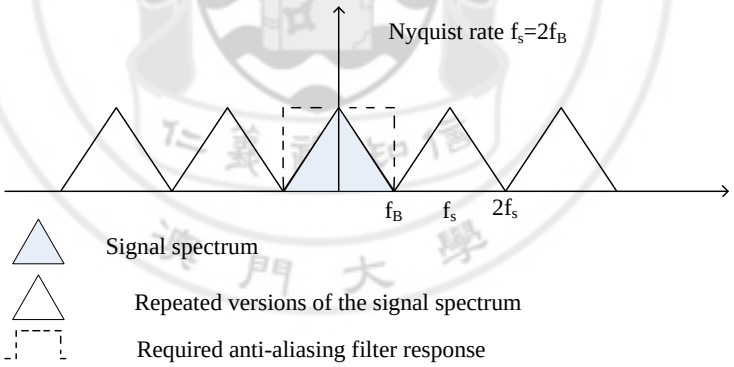



Figure 6 Nyquist sampling theory

In the sampling process, it is sampled at uniformly spaced time intervals T for a continuous time signal, The samples of the continuous time signal can be represented as x[n] = x(nT), where x[n] is the samples and x(t)is the continuous time signal. In the frequency domain, the effect of the sampling process is to create versions of the signal spectrum repeated at multiples of the sampling frequency = l/T periodically. [31]

## 2.2 Quantization

Amplitude quantization changes a sampled-data signal from continuous-level to discrete-level. The quantized output amplitudes are usually represented by a digital code word composed of a finite number of bits. The digital code words are often said to be in pulse code modulation (PCM) format. [3]

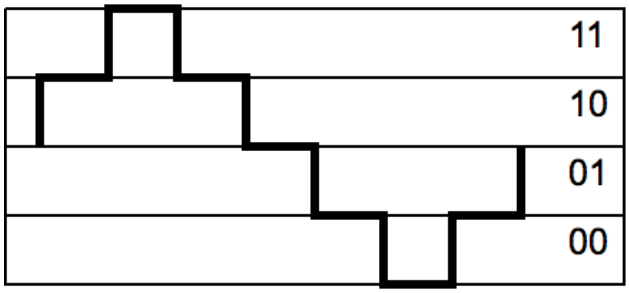



Figure 7 2-bit resolution with four levels of quantization of a sine wave

In analog-to-digital conversion, the difference between the actual analog value and quantized digital value is called quantization error or quantization distortion. This error is either due to rounding or truncation. The error signal is sometimes considered as an additional random signal called quantization noise. The power density spectrum is

$$p(\varepsilon_Q) = \begin{cases} \frac{1}{\Delta}, \ for\ \varepsilon_Q \in -\frac{\Delta}{2} \ldots\ldots \frac{\Delta}{2} \\ 0, \quad otherwise \end{cases} \tag{2}$$

And the error here is a white noise, the error sequence, e[n], is a sample sequence of a stationary random process. The quantization noise power is

$$P_Q = \int_{-\infty}^{\infty} {\varepsilon_Q}^2 . p(\varepsilon_Q)\, d\varepsilon_Q = \int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} \frac{{\varepsilon_Q}^2}{\Delta} d\varepsilon_Q = \frac{\Delta^2}{12} \tag{3}$$

- **Signal to noise ratio**

The effect of noise is quantified by the signal-to-noise ratio (SNR) defined by

$$SNR|_{dB} = 10log\frac{P_{sign}}{P_{noise}} \tag{4}$$

Where $P_{sign}$ and $P_{noise}$ are the power of the signal and the power of the noise in the band of interest.

Sine wave as example,

$$P_{sine} = \frac{1}{T}\int_0^T \frac{X_{FS}^2}{4} sin^2(2\pi ft)dt \approx \frac{1}{T}\int_0^T \frac{X_{FS}^2}{4}(2\pi ft)^2 dt = \frac{(\Delta \cdot 2^n)^2}{8} \quad (5)$$

And $P_Q = \frac{\Delta^2}{12}$

$$SNR_{sine}|_{dB} = (6.02 \cdot n + 1.78)dB \quad (6)$$

From the SNR equation, it can be concluded that every bit of the resolution improves the signal to noise ratio by 6.02 dB which is about 4 times improve.

## 2.3 Oversampling

Oversampling is the process of sampling a signal with a sampling frequency significantly higher than twice the bandwidth or highest frequency of the signal being sampled.

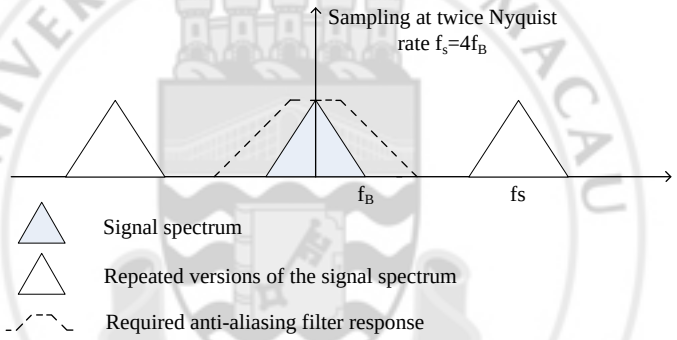



Figure 8 Sampling at twice the Nyquist rate

Another benefit directly caused by oversampling is that the requirement of the shape of the analog anti-aliasing filter can be decrease. It can be seen that a signal is sampled at twice the Nyquist rate in Figure 8. On this occasion, the anti-aliasing filter can have a transition band which is between fs/2 and $f_B$ if it can provides very good attenuation beyond fs/2

The SNR calculation on oversampling A/D converter: [4]

$$OSR = \frac{f_s}{2f_B} \quad (7)$$

In band noise power

$$\sigma_{ey}^2 = \int_{-f_B}^{f_B} P_{ey}(f)df = 2\int_0^{f_B} P_{ey}(f)df = \int_0^{f_B} \frac{2\sigma_e^2}{f_s} df = \sigma_e^2(\frac{2f_B}{f_s}) \quad (8)$$

Where $\sigma_x^2$ the input is signal power and define $OSR = 2^r$.

$$SNR = 10\,log\left(\frac{\sigma_x^2}{\sigma_{ey}^2}\right)$$

$$= 10\,log(\sigma_x^2) - 10\,log\left(\sigma_{ey}^2\right) + 3.01r \quad (9)$$

Every doubling of the OSR, the SNR improves by about 3dB which is one-half bit resolution improve.

All in all, Oversampling helps avoid aliasing, improves resolution, and reduces noise and the anti-aliasing filter dose net need as sharp a cutoff.

## 2.4 Noise Shaping

Noise shaping is a technique which reduces the in-band noise by incorporating in a feedback loop, which is the one of the key technique on the sigma delta ADC.

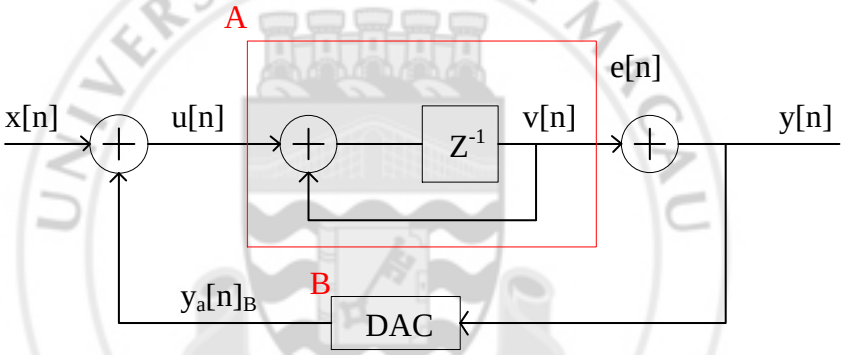



Figure 9 Block diagram of Sigma-Delta modulation [29]

From the block diagram, the noise transform function can be found

$$[X - Y \cdot B(z)]A(z) + \varepsilon_Q = Y$$

$$Y = \frac{X \cdot A(z)}{1 + A(z)B(z)} + \frac{\varepsilon_Q}{1 + A(z)B(z)}$$

$$NTF(z) = \frac{Y}{\varepsilon_Q} = \frac{1}{1+A(z)B(z)} \quad (10)$$

Where $A(z) = \frac{z^{-1}}{1-z^{-1}}$ and $B(z) = 1$

Therefore the noise transform function is

$$NTF(z) = 1 - z^{-1}$$

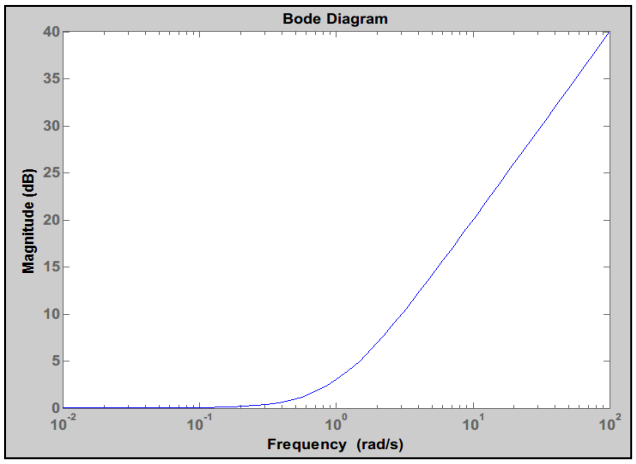



Figure 10 Bode plot of noise transform function

In the Bode plot of the 1st order NTF above, it shows the shape of the NTF with the slop about 20dB/ decade. The distribution of the noise change which cause the in band noise decrease. The noise shape after each operation can be describe as following.

Then the corresponding SNR can be calculated:

$$Y(z) = X \cdot STF(z) + \varepsilon_Q(z) \cdot NTF(z) \tag{11}$$

Where:

$$STF(z) = Z^{-1}$$

$$NTF(z) = 1 - Z^{-1}$$

$$NTF(\omega) = 2je^{-j\omega T/2} sin(\omega T/2) \tag{12}$$

In-band noise power,

$$P_{ey}(f) = P_e(f)|NTF(f)|^2 = \frac{\sigma_e^2}{f_s} \cdot 4 \cdot sin^2(\pi f) \tag{13}$$

$$\sigma_{ey}^2 = \int_{-f_B}^{f_B} P_{ey}(f)df = 2\int_0^{f_B} P_{ey}(f)df$$

$$= \sigma_e^2 \cdot \frac{\pi^2}{3} \cdot \left(\frac{2f_B}{f_s}\right)^3 \tag{13}$$

The corresponding SNR is

$$SNR = 10\log\left(\frac{\sigma_x^2}{\sigma_{ey}^2}\right) = 10\log(\sigma_x^2) - 10\log\left(\sigma_{ey}^2\right) + 10\log\left(\frac{\pi^2}{3}\right) + 9.03r \tag{14}$$

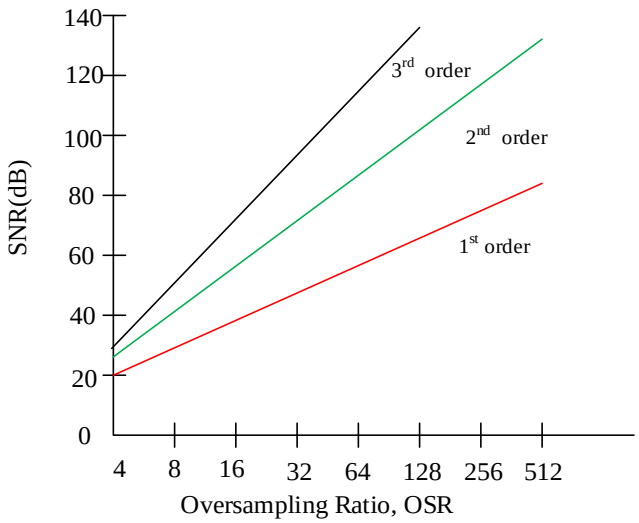



Figure 11 SNR vs OSR for sigma delta modulation

From equation of SNR above, if oversampling ratio is double which means increase the r the SNR improves about 9 dB, and the resolution increase about 1.5 bits equivalently. That is better than the Nyquist ADC.

For the second order, if the oversampling ratio is double the SNR will increase about 15dB. Moreover the SNR performance of sigma delta modulation can increase about 21dB if the oversampling ratio is double for the third order modulation.

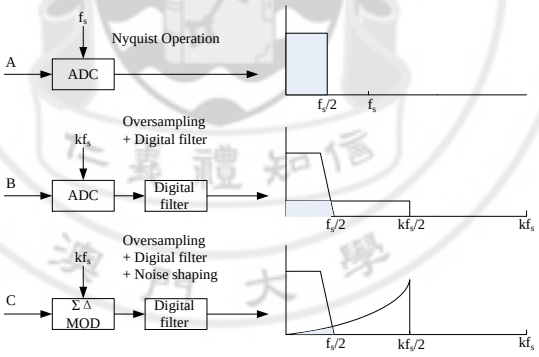



Figure 12 Each operation of sigma delta ADC

## 2.5 Digital Decimator

The digital decimator consists of low pass filter and down sampler, the usages of the decimator:

- Filter the noise after noise shaping
- Anti-aliasing, cancel the out-band noise
- Reduce the ADC data rate of output

This one is not needed for our design, which will be talked later.

# III TARGET SPECIFICATION

In order to design the system as well as the further circuit of this project, setting the target specification is necessary after known the sigma-delta technique (oversampling and noise shaping) and its characteristic.

In this project, the target is to design a high performance ΣΔ ADC in audio application. The specification should be basic on the audio application. For different application, the ADCs have different requirement.

In general, it separate the products as the 'home audio', 'portable audio' and 'professional audio'. [40] The products that mostly draw people attention must be portable product such as mobile phone, mp3. And the high quality audio portable product is required in car audio system because of the closed environment of the car. So we want to design a sigma-delta ADC for the car audio system which is similar to the home hi-fi system. The following part is the specification of some actual products from different company, which is a good reference to make further decision about the specification.

Table 2 Audio Sigma-Delta Adc From Ti [40]

| | SNR | sampling rate(max) | power (chip) |
|---|---|---|---|
| pcm1802 | 105dB | 96kHz | 147mW |
| pcm1803a | 103dB | 96kHz | 60mW |
| pcm1804 | 111dB | 96kHz | 225mW |
| pcm1804-q1 | 112dB | 192kHz | 225mW |
| pcm1807 | 99dB | 96kHz | 62mW |
| pcm1808 | 99dB | 96kHz | 62mW |
| pcm1808-q1 | 99dB | 96kHz | 62mW |
| pcm1851a | 101dB | 96kHz | 160mW |
| professional | | | |
| PCM4202 | 118dB | 216KHz | 308mW |
| PCM4204 | 118dB | 216KHz | 600mW |
| PCM4220 | 123dB | 216KHz | 305mW |
| portable | | | |
| PCM4201 | 112dB | 108KHz | 49mW |
| PCM1870A* | 90dB | 50KHz | 40mW |
| tlv320adc3001 | 96dB | 96KHz | 17mW |

From the table, the pcm1808 are the audio ADCs use in car audio system. The SNR performance is 99dB.

Table 3 Automotive Audio ADC Product Of ADI And AKM [2]

| | Bits | Max fs(kHz) | S/N(dB) |
|---|---|---|---|
| AK5355VN | 16 | 50 | 91 |
| AK5355VT | 16 | 50 | 91 |
| AK5357KT | 24 | 96 | 102 |
| AK5357VT | 24 | 96 | 102 |
| AK5359VT | 24 | 216 | 102 |
| AK5381VT | 24 | 96 | 106 |
| AK5384VF | 24 | 96 | 107 |
| AK5385BVF | 24 | 216 | 114 |
| AK5386VT | 24 | 216 | 110 |
| AK5701KN | 16 | 48 | 89 |
| AK5730VQ | 24 | 48 | 100 |
| ADI | | | |
| AD1871 | 24 | 96 | 105 |
| AD1877 | 16 | 48 | 94 |
| ADAU1977 | 24 | 192 | 106 |
| AD1974 | 24 | 192 | 105 |

From the two table above, the SNR performance of the ADCs are usually greater than 100dB. Moreover, the target of this project is to design a higher performance one. Therefore, we set our target of the SNR performance to 105dB. After setting the target, the structure of the ΣΔ ADC will be chosen to build the system so that we can achieve our target. The difference between each structure will discusses in following part.

# IV MODELING TECHNIQUE

## 4.1 Conventional Modulator Structure

To choose the structure, the basic of different structure modulators should be learnt. Here start from the conventional second order modulator which are basic and easier to understand and simulate. [38]

### A. The Boser-Wooley Modulator

A second-order modulator with two delaying integrators is called the Boser-Wooley modulator. [36]

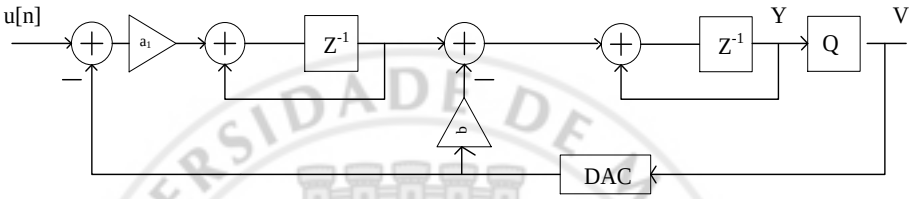
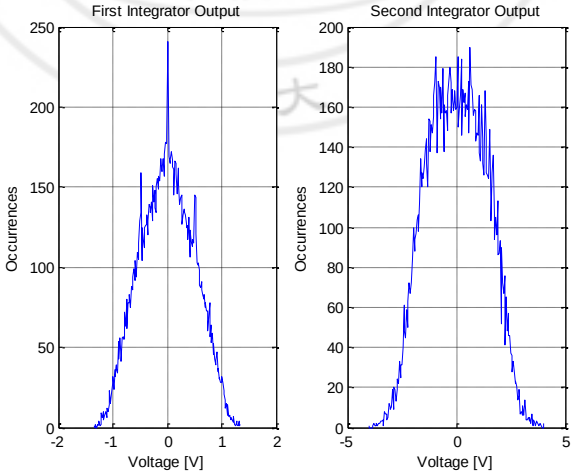



Figure 13 The Boser-Wooley modulator

$\mathrm{STF(z)} = \frac{a_1 a_2 z^{-2}}{D(z)}$ and $\mathrm{NTF(z)} = \frac{(1-z^{-1})^2}{D(z)}$

$$\mathrm{D(z)} = (1 - Z^{-1})^2 + a_2 \mathrm{b} Z^{-1}(1 - Z\text{^}(-1)) + a_1 a_2 Z^{-2} \qquad (15)$$

The parameter $a_1a_2$=1 and $a_2$b=2, then use the example in the book to build the Matlab model. In the actual design process, dynamic range scaling removes any ambiguity in finding the parameters needed to implement a given NTF and STF.



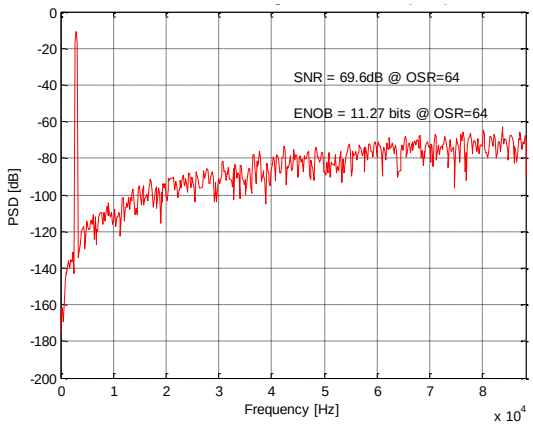



Figure 14 The simulation model of Boser-Wooley modulator with a1=0.5 a2=2 and b=1 using single bit quantizer

It allows the op amps in each integrator to settle independently of each other, thereby relaxing their speed requirements. It has two feedback paths, two signal feedback into the each input of the integrator. Therefore, the swing of output of integrator is high.

## B. The Silva-Steensgaard Structure

The Silva-Steensgaard Structure actually is a second order modulator with feed-forward paths. The distinguishing features of this circuit are the direct feed-forward path from the input to the quantizer and the single feedback path from the digital output linear analysis confirms that the output is given in the z-domain by as before.

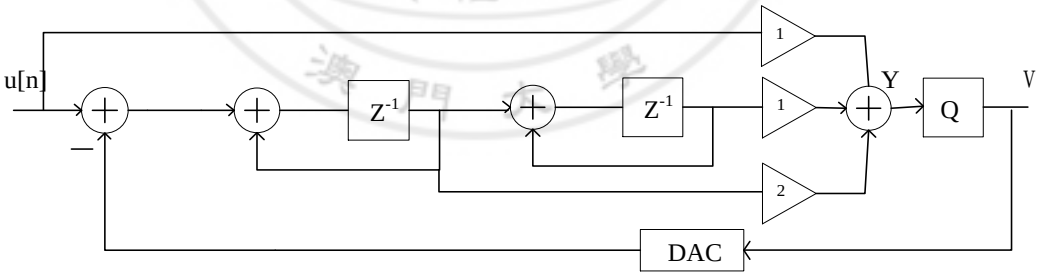



Figure 15 The Silva-Steensgaard Structure

$$V(z) = U(z) + (1 - z^{-1})^2 E(z) \quad (16)$$

The input signal to the loop filter is, however, different: it contains only the shaped quantization noise:

$$U(z) - V(z) = -(1 - z^{-1})^2 E(z) \quad (17)$$

Also, use the single bit quantizer to build the simulation model.

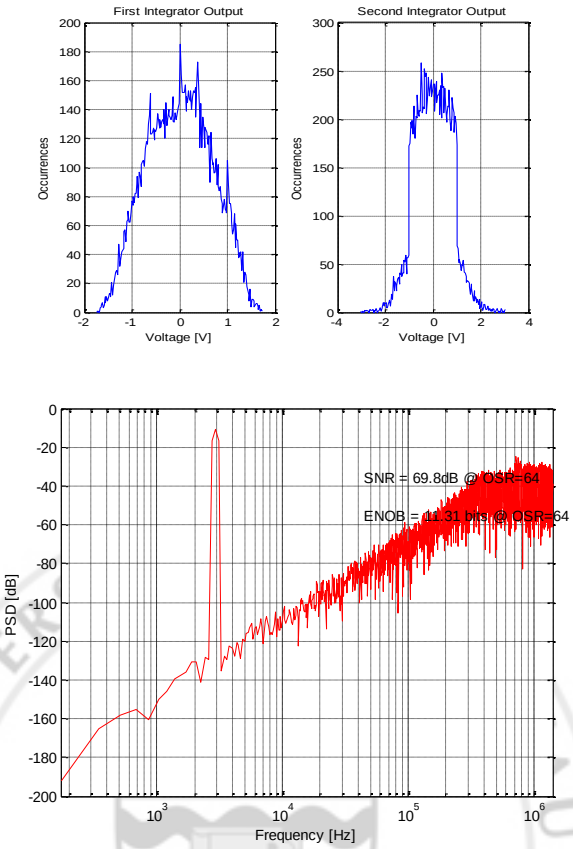



Figure 16 The simulation circuit of Silva-Steensgaard Structure

Since the loop filter thus does not need to process the signal, the requirements on its linearity may be greatly reduced, which is a significant practical advantage. And it only has one feedback the power consumption and the swing will not such high. However, it needs a very high accuracy of the adder.

## C. The Error-Feedback Structure

Here is the structure of the error-feedback: [36]

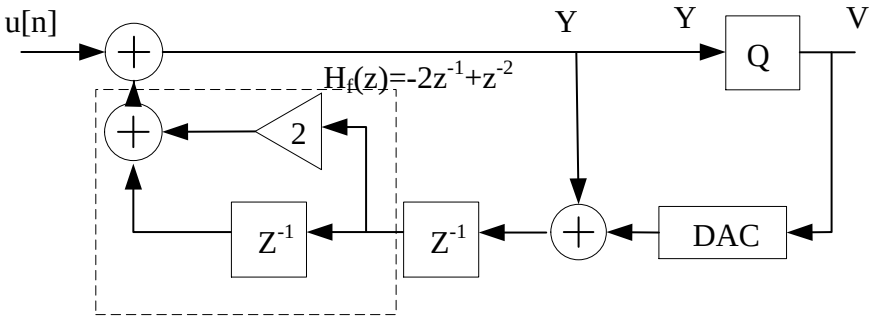



Figure 17 Error-Feedback Structure

$$NTF = 1 + H_f(z)$$

To obtain

$$NTF = (1 - z^{-1})^2$$

The H (f) should be

$$H_f(z) = (1 - z^{-1})^2 - 1 = -2z^{-1} + z^{-2} \quad (18)$$

Use the single bit quantizer to build the simulation model. And this example looks simple and hence attractive, but it is impractical for the analog sigma delta loops. We can see the reason in the simulation performance.

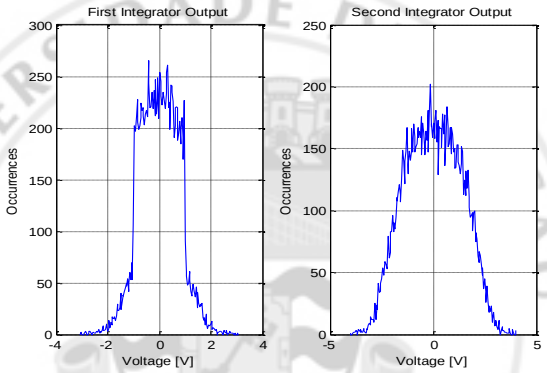



Figure 18 The simulation circuit of Error-Feedback Structure

In practice, even with careful analog design, the achievable ENOB will typically be less than 10 bits for ADCs with a single-bit quantizer, even for high OSR.

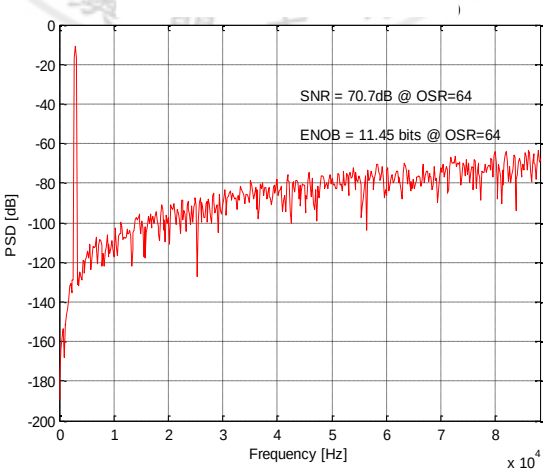



Figure 19 SNR performance of Error Feedback

For this structure, it is not practical for analog implementation, since it is very sensitive to variations of its parameters.

Table 4 The SNR As The Coefficient Changes.

| Coefficient | SNR(dB) |
|---|---|
| 2 | 70.7 |
| 2.001(0.05%) | 64.8 |
| 2.002(0.1%) | 61.7 |

### D. Summary

In a partly conclusion, this examined the second-order modulator, MOD2 and several of its variants. Like MOD1, MOD2 is theoretically able to achieve high resolution for inputs, and is immune to a variety of imperfections. In contrast to MOD1, which displays a 9 dB increase' in SQNR for every doubling of OSR, the SQNR of MOD2 increases at 15 dB per octave. As a result, MOD2 is able to achieve a high level of performance with a lower over sampling ratio than MOD1would require. Due to the gain-squaring provided by the two-integrator cascade, MOD2 is also more robust in the face of finite op-amp gain than MOD1. Moreover, the quantization noise at the output of MOD2 is less likely to contain tones than the noise at the output of MODI. In all these areas, MOD2 is markedly superior to MOD1. The primary drawbacks associated with MOD2 are increased hardware requirement (both analog and digital) and decreased the allowable signal range.

## 4.2 Advanced Modulator Structure

### A. CIFB (Cascade Of Integrators With Distributed Feedback)

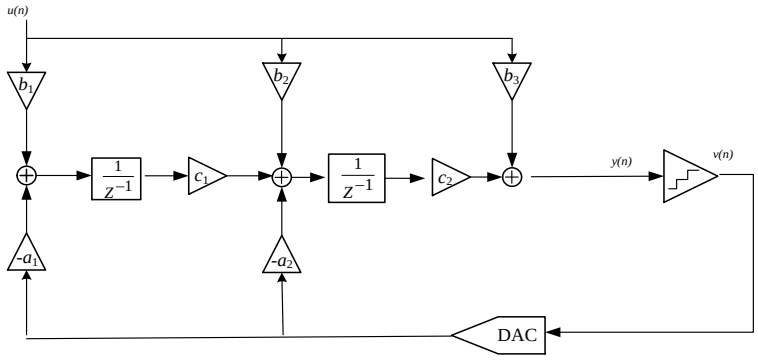



Figure 20 The CIFB Structure

$$L_0(z) = \sum_{i=1}^{N+1} \frac{b_i}{(z-1)^{N+1-i}} \quad (19)$$

And the L1 is

$$L_1(z) = \sum_{i=1}^{N} \frac{-a_i}{(z-1)^{N+1-i}} \tag{20}$$

According to the general structure

$$\mathrm{NTF(z)} = \frac{1}{1-L_1(z)} = \frac{(z-1)^N}{D(z)} \tag{21}$$

$$\mathrm{STF(z)} = \frac{L_0(z)}{1-L_1(z)} = \frac{b_1+b_2(z-1)+\cdots+b_{N+1}(z-1)^N}{D(z)} \tag{22}$$

- Feedback coefficients a's realize the zeroes of L1 and thus the NTF and STF poles.
- Feed-in coefficients b's determine zeroes of L0 and thus the STF zeroes.
- State scaling coefficients c's are used for dynamic range scaling.
- Implements Butterworth NTF.

Build the 2nd order model as example with single bit quantizer:

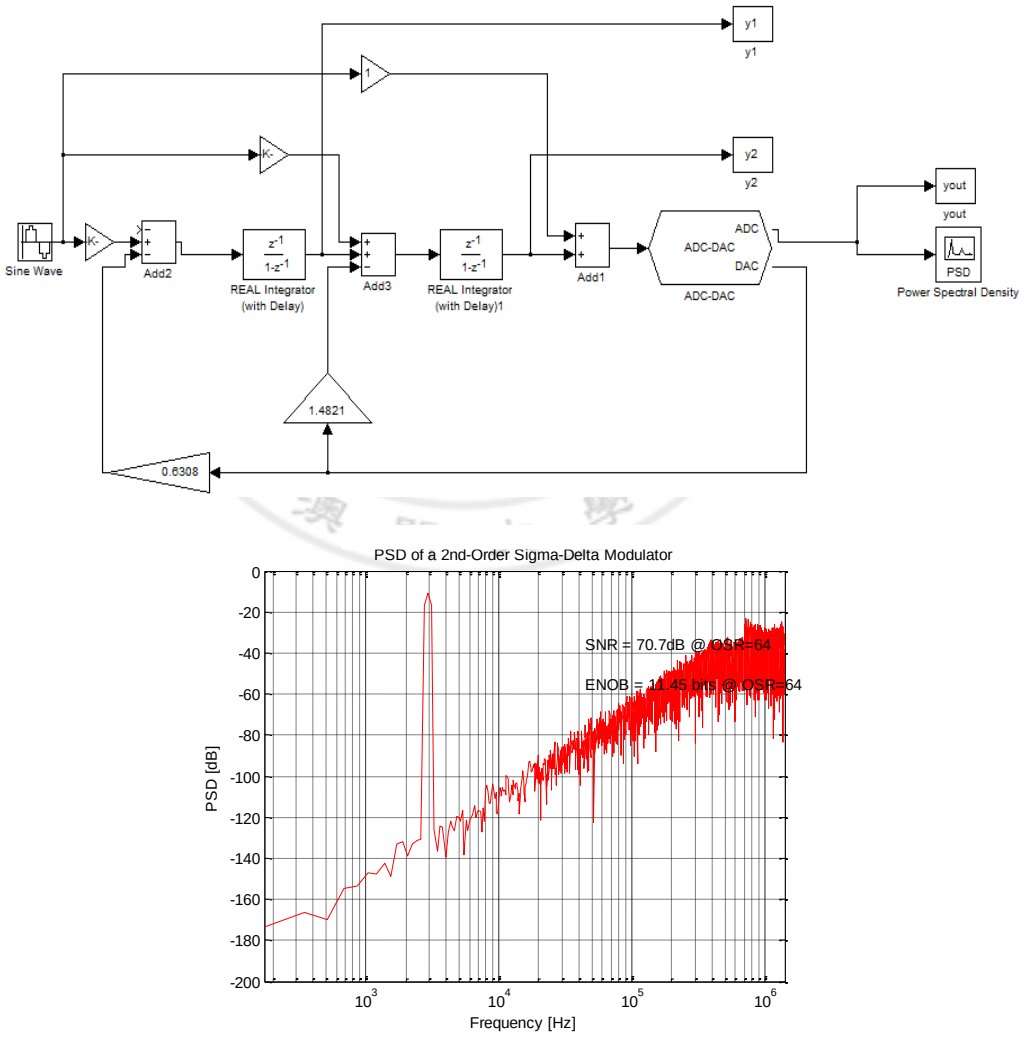



Figure 21 The simulation circuit of 2nd CIFB Structure (OSR=64)

## B. CIFF (Chain of Integrators with Feed-Forward summation)

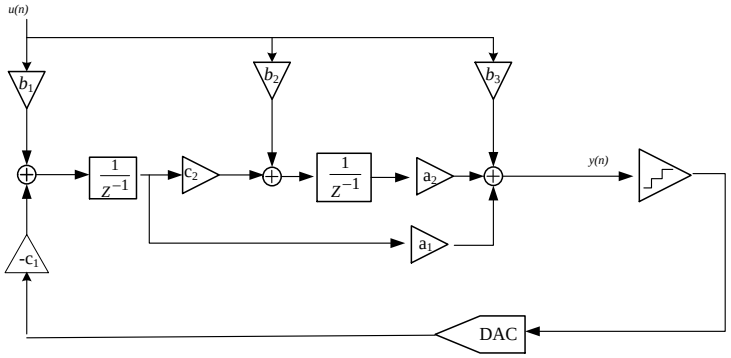



Figure 22 The CIFF structure

Instead of using a feedback structure to realize the loop-filters L0 and L1 given by Equations mentioned last, a feed-forward structure can also be employed. Figure 1 shows a third-order modulator with delaying integrators and feed-forward branches. This topology is called Chain of Integrators with Feed-Forward summation (CIFF).

We can observe that the feedback filter transfer function is given

$$L_1(z) = \sum_{i=1}^{N} \frac{-a_i}{(z-1)^{N+1-i}} \tag{23}$$

Similarly, the input transfer function is given

$$L_0(z) = \frac{r_1 + r_2(z-1) + \cdots + r_N(z-1)^{N-1} + r_{N+1}(z-1)^N}{(z-1)^N} \tag{24}$$

Where

$$r_1 = b_1 a_N \qquad r_N = b_1 a_1 + b_2 a_2 \ldots\ldots \qquad r_{N+1} = b_{N+1} \tag{25}$$

There are some typical cases

$$b_2 = b_3 = \cdots = b_N = 0 \; and \; b_1 = b_{N+1} = 1$$

$$L_0(z) = 1 - L_1(z)$$

Further, when $b_{N+1} = 1$

$$L_0(z) = 1 - L_1(z)$$

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} = 1 \tag{26}$$

$$NTF(z) = \frac{1}{1 - L_1(z)} \tag{27}$$

And when $b_{N+1} = 0$

$$L_0(z) = -L_1(z)$$

$$STF(z) = 1 - NTF(z) = \frac{-L_1(z)}{1-L_1(z)} \quad (28)$$

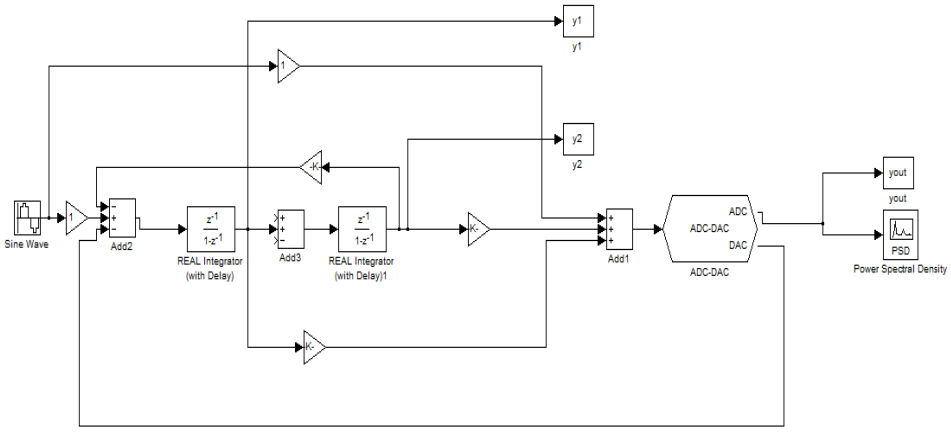
$$NTF(z) = \frac{1}{1-L_1(z)} \quad (29)$$

Cascade of delaying integrators:

- Feedforward coefficients a's realize the zeroes of L1 and thus the NTF and STF poles.
- Feed-in coefficients b's determine zeroes of L0 and thus the STF zeroes.
- State scaling coefficients c's are used for dynamic range scaling.

The 2nd order model as example, the simulation of CIFF is done with resonator. Uses resonators formed with two delaying integrators. Resonator poles outside the unit circle

$z_i = e^{1 \pm j\sqrt{g_1}}$



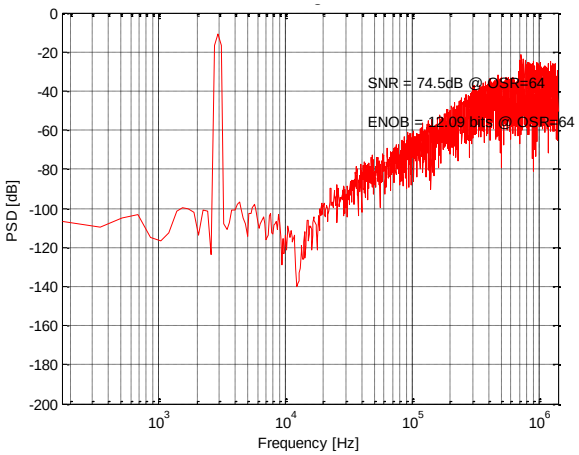



Figure 23 The simulation circuit of 2nd order CIFF Structure with resonator

## C. CRFB (Cascade of Resonators with Distributed Feedback)

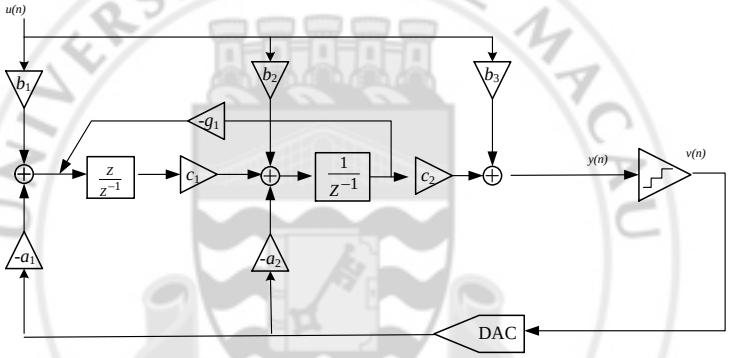



Figure 24 The CRFB Structure

Characteristic of this structure:

- Combine a non-delaying and a delaying integrator with local feedback around them, to form a stable resonator.
- Local feedback coefficients g's realize the complex zeroes in the NTF.
- Implements NTF with complex zeroes.
- For odd-order, use an integrator in the front to avoid noise coupling due to g.

To know how the g realize the complex zeroes in the NTF, I analyze the resonator.

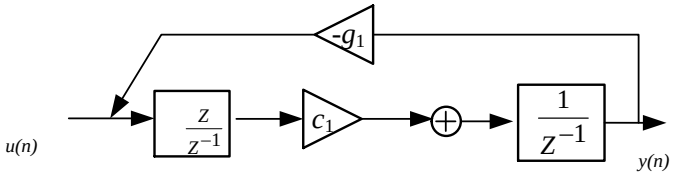



Figure The resonator Structure

Original:

$$Y(z) = \frac{z}{(z-1)^2} U(z) \tag{30}$$

$$H(z) = \frac{Y(z)}{U(z)} = \frac{z}{(z-1)^2} \tag{31}$$

Poles: z=1; Resonator:

$$Y(z) = \frac{z}{(z-1)^2} U(z) - \frac{gz}{(z-1)^2} Y(z) \tag{32}$$

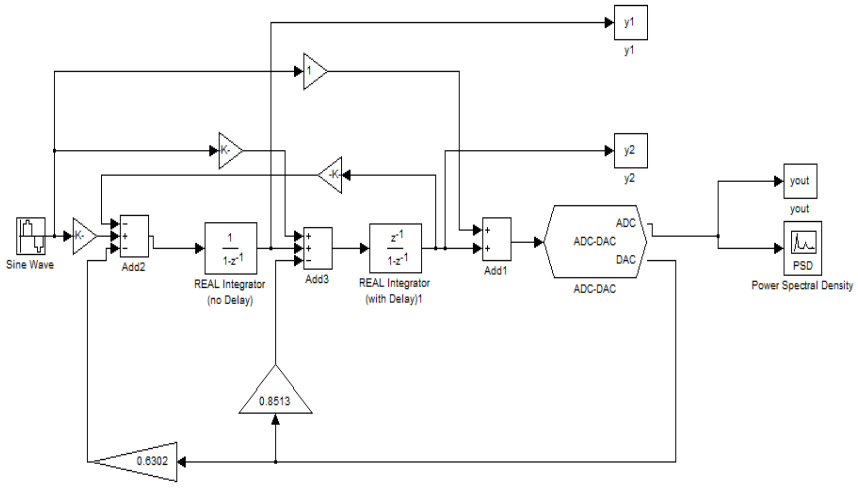
$$R(z) = \frac{Y(z)}{U(z)} = \frac{z}{z^2 - (2-g)z + 1}$$

$$= \frac{z}{(z-e^{j\alpha})(z-e^{-j\alpha})} \tag{33}$$

Where $\alpha = cos^{-1}(1 - \frac{g}{2})$ and $\sin\left(\frac{\alpha}{2}\right) = \pm\frac{\sqrt{g}}{2}$

$$\alpha \approx \pm\sqrt{g} \tag{34}$$

The poles become $z = e^{\pm j\sqrt{g}}$ actually is the zeros of NTF. Build the 2nd order model as example,



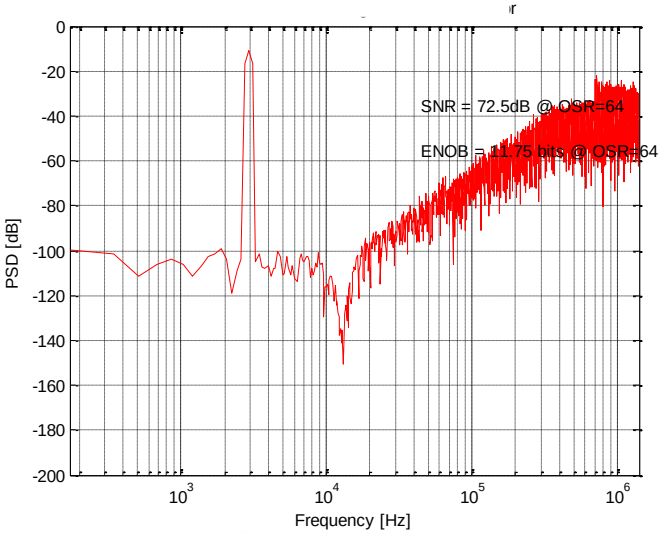



Figure 25 The simulation circuit of 2nd order CRFB Structure

**CRFB Without Delay**

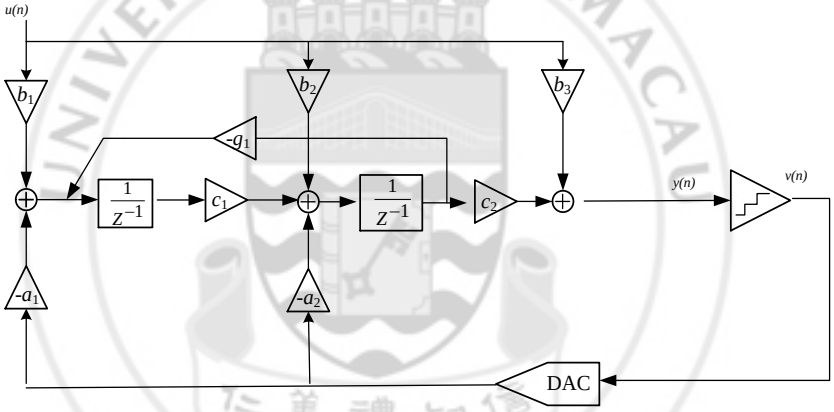



Figure 26 The CRFB Structure without delay

Characteristic of this structure:

- A resonator can also be formed with two delaying integrators
- Resonator poles outside the unit circle.
- Locally unstable but works fine in a stable loop-filter.
- Relaxes settling requirements on the op-amps and implements complex NTF zeroes.

Also, analyze the resonators

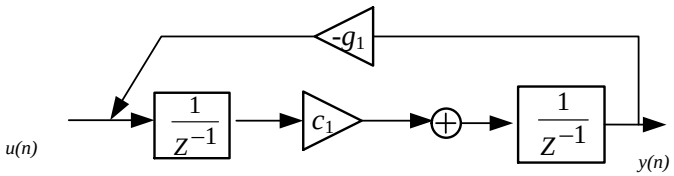



Figure 27 The resonator Structure without delay

Original:

$$Y(z) = \frac{1}{(z-1)^2} U(z) \tag{35}$$

$$H(z) = \frac{Y(z)}{U(z)} = \frac{1}{(z-1)^2} \tag{36}$$

Poles: $z = 1$

Resonator:

$$Y(z) = \frac{1}{(z-1)^2} U(z) - \frac{g}{(z-1)^2} Y(z) \tag{37}$$

$$R(z) = \frac{Y(z)}{U(z)} = \frac{1}{z^2-2z+g+1} \tag{38}$$

Where $\tan(\alpha) = \pm\sqrt{g}$ and $\alpha \approx \pm\sqrt{g}$

Poles:

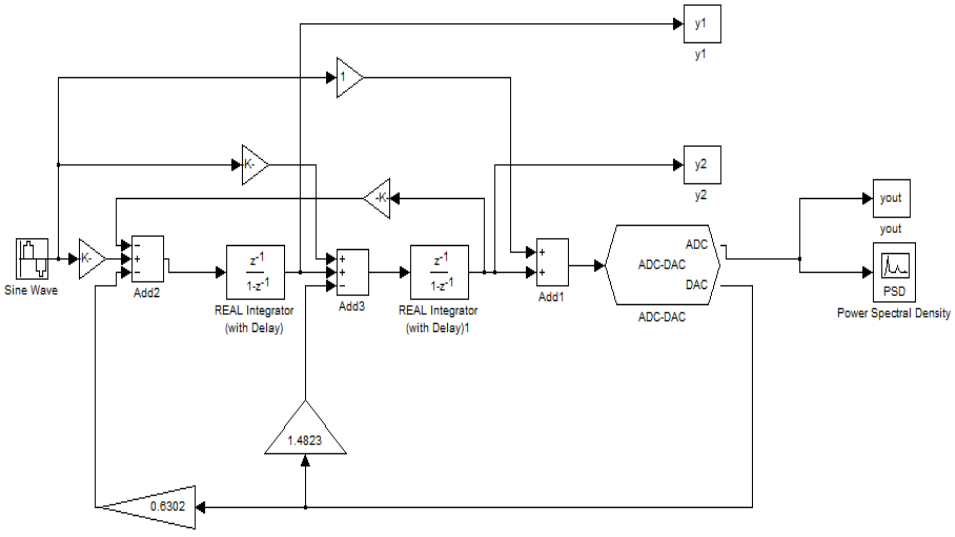
$$z = 1 \pm j\sqrt{g} \tag{39}$$

Which are out of the unit circle.

Table 5 The SNR of different structure with single bit quantizer

| | CIFB | CRFB(without delay) | CRFB |
|---|---|---|---|
| SNR | 70.7dB | 74.5dB | 72.5dB |

Therefore, if the SNR is the only consideration, the CRFB structure without delay is better than the others. Build the 2nd order model as example,



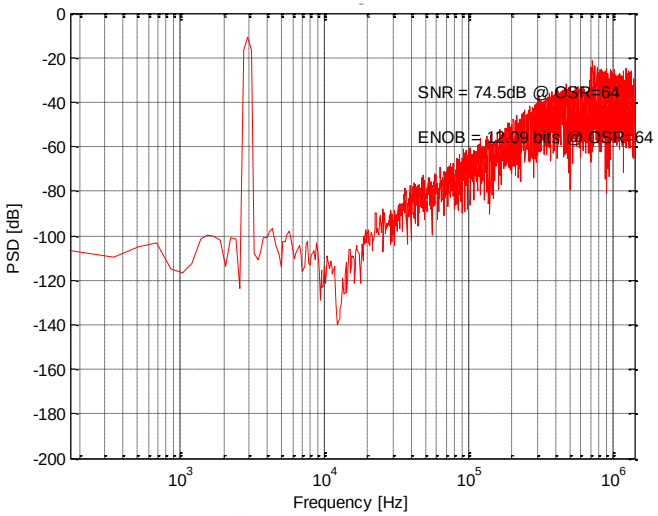



Figure 28 The simulation circuit of 2nd order CIFB Structure with resonator

## D. CRFF

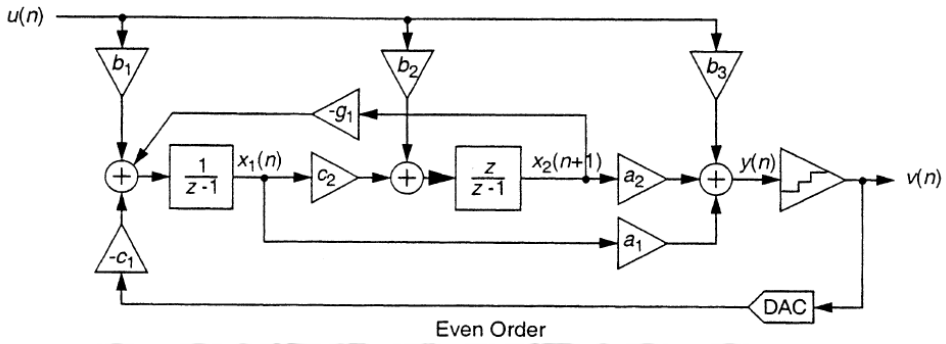


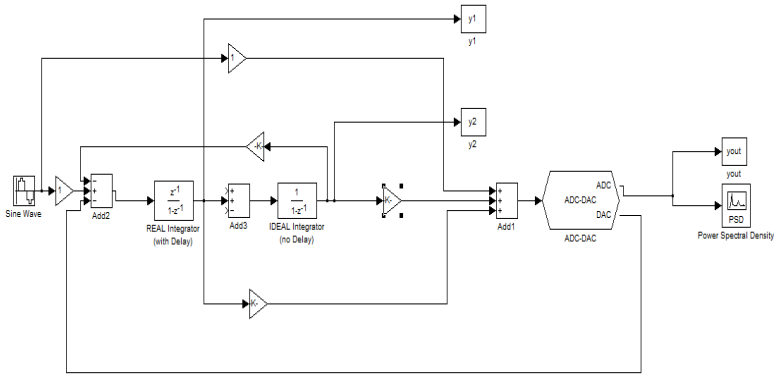

Figure 29 The CRFF structure

To obtain optimized zeroes for H (z), resonators must be created by internal feedback within the loop filter (Figure 29). Use resonators with feed-forward summation.

- Local feedback coefficients g's realize the complex zeroes in the NTF.
- Implements NTF with complex zeroes.(zero optimize)

$$(z_i = e^{\pm j\sqrt{g_1}}) \qquad (40)$$

For odd-order, use an integrator in the front to avoid noise coupling due to g. Build the 2nd order model as example,



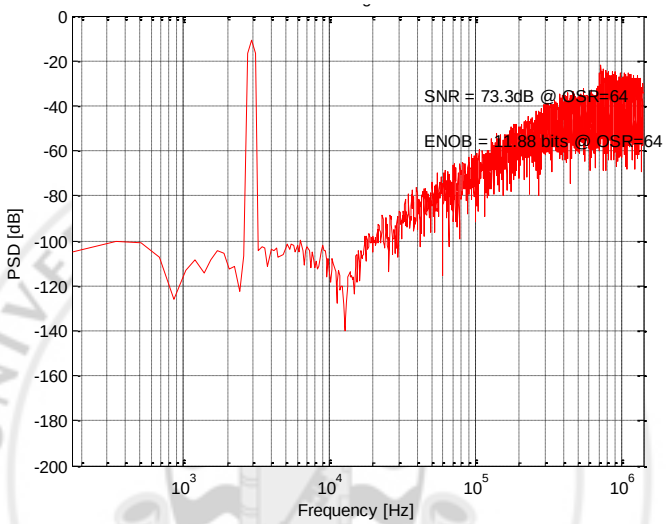




Figure 30 The simulation result of 2nd order CRFF structure

## E. Comparison

Table 6 Comparison Between Feed Forward And Feedback Structure.

| Feedforward | Feedback |
|---|---|
| Has relaxed dynamic range requirements | Integrator output contain significant amount of input signal as well as filter quantization noise |
| Only one DAC required | Requires many feedback DACs |
| Needs an extra adder | No extra adder |
| First integrator is fastest | Last integrator is fastest |
| First opamp is power hungry | First opamp is power hungry |
| Small capacitor area | Large capacitor area to accommodate the large signal swings. |

Advantages of Feedforward compared to Feedback: Lower signal swing at the output of the integrators (beneficial for amplifier design), larger first loop filter coefficient (better noise suppression than feedback structure), single DAC only, and depending on the implementation the feedforward structure might recover from instability without additional circuitry. The disadvantage of the feedforward structure is that the extra summing node in front of the quantizer should be very accuracy.

In general, I think that the lower signal swing is the main motivation why feedforward structures are preferred nowadays. But in this project feedback structure is chosen for the simple adder.

## 4.3 Multi-Stage Modulation

The world of noise-shaping converters can be roughly divided into single-bit single-loop low-order designs, single-bit single-loop high-order designs, multi-loop cascaded designs with feed-forward error cancellation, and multi-bit noise shapers. In this report, the multi bit will be not mentioned.

### A. The Leslie-Singh (L-0 Cascade) Structure

A simple two-stage delta-sigma ADC contains an L-th order delta-sigma modulator as its first stage, and a static (i.e., zero-order) ADC as its second stage. The outputs of the two stages, v1 and v2 are digitally filtered and combined to obtain the overall output v.

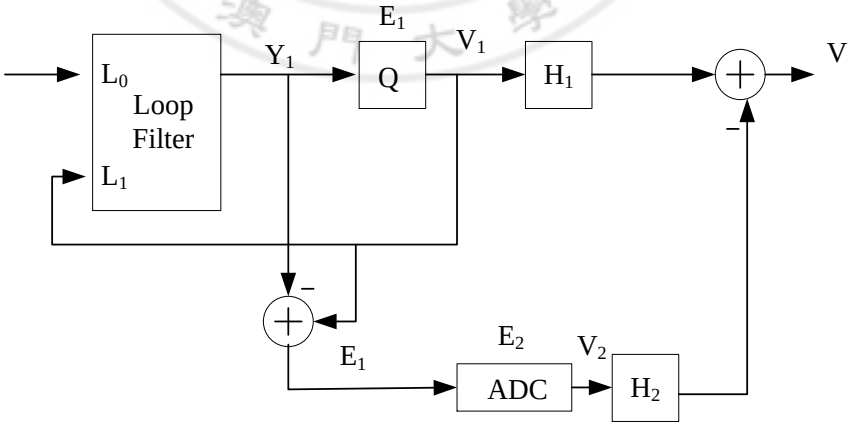



Figure 31 The L-0 cascade (Leslie-Singh) structure

As shown, the quantization error e1 (n) of the input stage is extracted in analog form by subtracting the input signal y1 of the internal quantizer from its output v1.

$$V(z) = V_1(z)H_1(z) - V_2(z)H_2(z) \tag{41}$$

Usually H1 implements the latency of the second ADC:

$$H_1 = z^{-k}$$

$$\mathrm{V(z)} = \mathrm{z^{-k}[STF_1(z)U(z) + NTF_1(z)E_1(z)] - NTF_1(z)\{z^{-k}[E_1(z) + E_2(z)]\}}$$

$$= \mathrm{z^{-k}[STF_1(z)U(z) - NTF_1(z)E_2(z)]} \tag{42}$$

Comparing the output V (z) with the first-stage output V1 (z). NTF1 shapes now the q-error of the second stage, which can be made much smaller than the q-error of the first stage because the second stage has no feedback, no delay issues and it can be implemented as multi-bit such as pipeline ADC which is easier than a multi-bit loop quantizer in the first stage. Hence, this technique can enhance the SQNR by as much as 25~30 dB.

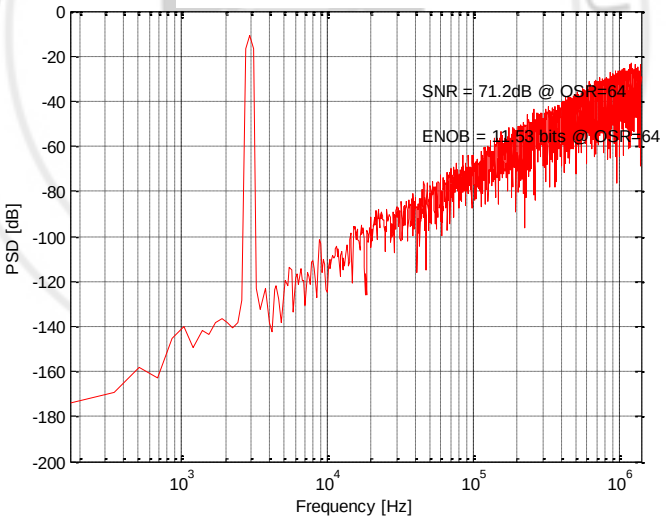



Figure 32 Simulation result of the 2-0 cascade (Leslie-Singh) structure

Further, to avoid the subtraction altogether, the input signal of the second stage can be chosen as y1 (n), the input signal of the first-stage ADC, instead of e1 (n).

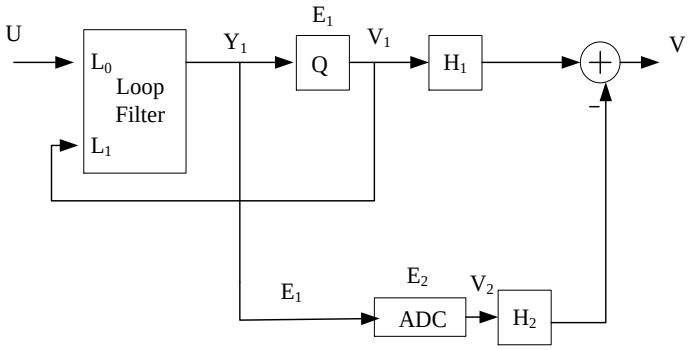



Figure 33 The L-0 cascade (Leslie-Singh) structure

$$Y_1(z) = V_1(z) - E_1(z) \tag{43}$$

Keeping the H1=z-k but choosing $H_2(z) = \frac{NTF_1(z)}{NTF_1(z)-1}$

Finally,

$$V(z) = \frac{z^{-k}STF_1(z)}{1-NTF_1(z)}U(z) + \frac{z^{-k}NTF_1(z)}{1-NTF_1(z)}E_2(z) \tag{44}$$

In signal band, |NTF1|<<1, and hence the SQNR obtained with the new V (z) is very close to the one obtained with the V (z) mentioned before.

A disadvantage is that y1 (n) contains the signal u (n) as well. Hence, the second ADC must be able to handle much larger signals and must have a much higher linearity!

## B. MASH Modulator

An obvious extension of the Leslie-Singh modulator, which historically preceded it, is the cascade modulator, also called multi-stage or MASH (for Multi-stage noise-Shaping) modulator. Here, the second stage is realized by another delta-sigma modulator.

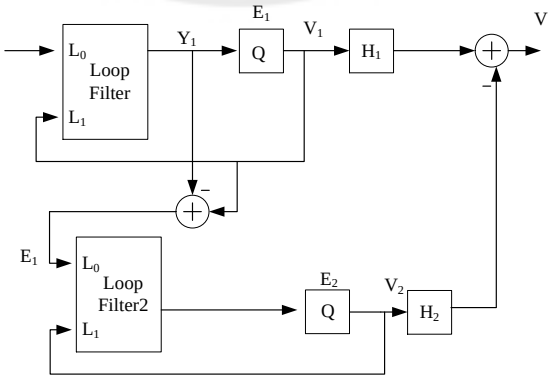



Figure 34 A MASH structure

As Figure 34 shown, e1 (the quantization error) of the input stage is found in analog form by minus the input to its internal quantizer from its output.

$$V_1(z) = STF_1(z)U(z) + NTF_1(z)E_1(z) \quad (45)$$

$$V_2(z) = STF_2(z)U(z) + NTF_2(z)E_2(z) \quad (46)$$

Moreover,

$$V(z) = V_1(z)H_1(z) - V_2(z)H_2(z) \quad (47)$$

To cancel the E1 (z), it is required that

$$H_1(z)NTF_1(z) = H_2(z)STF_2(z) \quad (48)$$

The overall output,

$$V(z) = STF_1(z)STF_2(z)U(z) - NTF_1(z)NTF_2(z)E_2(z) \quad (49)$$

A typical case is a MASH with two 2nd -order modulators (2-2 MASH)

$$STF_1(z) = STF_2(z) = z^{-2} \quad (50)$$

$$NTF_1(z) = NTF_2(z) = (1 - z^{-1})^2 \quad (51)$$

$$V(z) = z^{-4}U(z) - (1 - z^{-1})^4E_2(z) \quad (52)$$

Noise shaping performance of a 4th -order single-loop modulator, but stability of a 2nd -order modulator.

Here are some simulation results of different MASH structure.

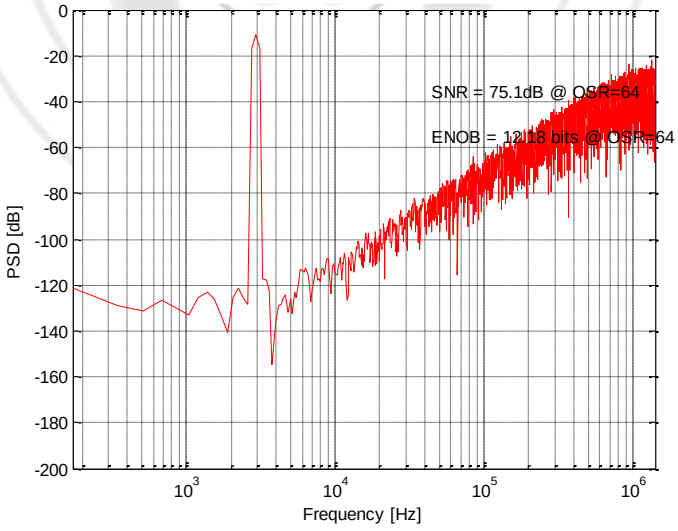



Figure 35 Simulation result of the 1-1 MASH structure

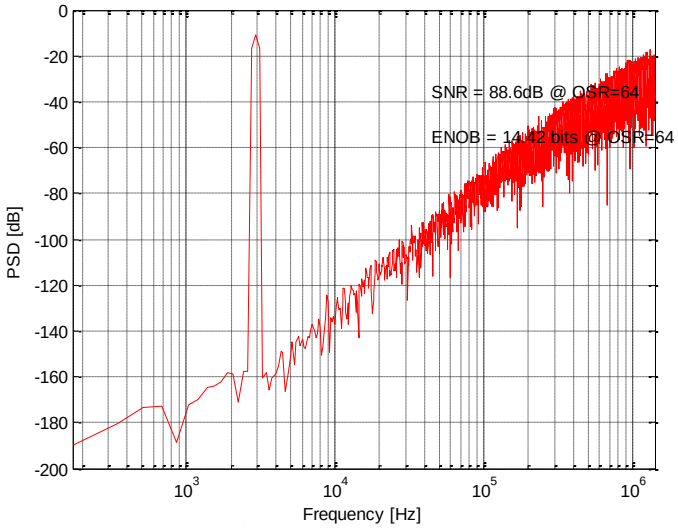



Figure 36 Simulation result of the 2-1 MASH structure

As the order of first stage increases, the SNDR performance is better. Further, the 3-stage and 4-stage structure

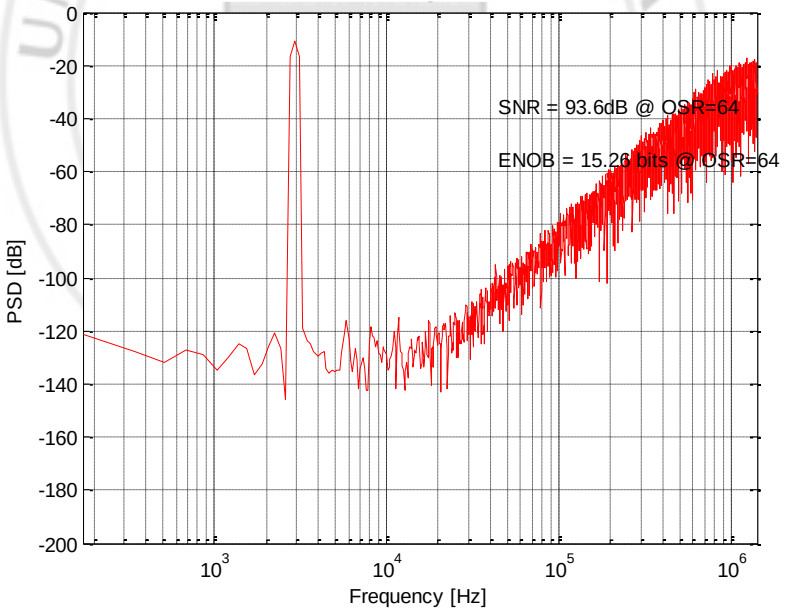



Figure 37 Simulation result of the 1-1-1 MASH structure

As shown, the SNDR performance as well as the stability performance of 3-stage (1-1-1) MASH is better than 3-stage (2-1).

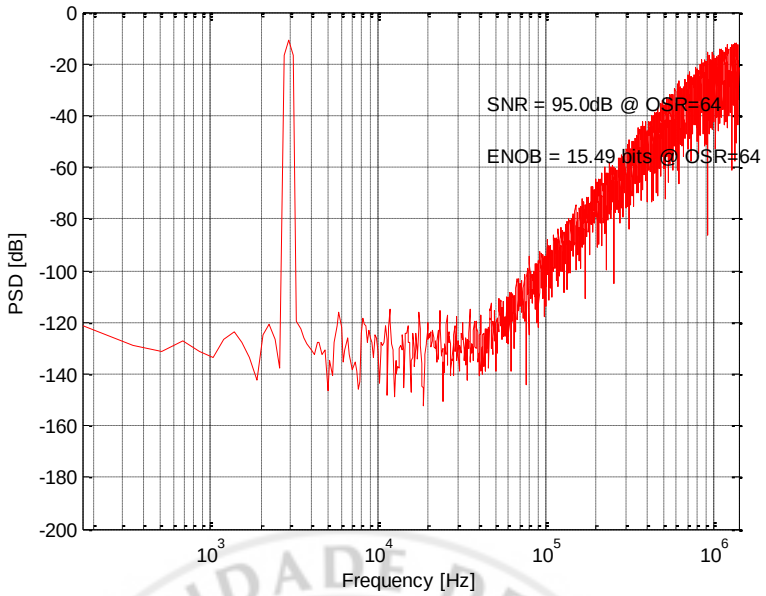



Figure 38 Simulation result of the 1-1-1-1 MASH structure

As shown, the SNDR(95 dB) performance is better as the stage increase.

The Multi-loop cascade has the advantages of low-order single-loop single-bit which are the higher stability. Also it has the higher SNR performance. But the multi-loop cascade has to near perfect matching between analog integrator and digital differentiator. It has high requirement in the switching-capacitor circuit.

## 4.4 Analysis

Single-loop high-order designs are most attractive whenever high SNR, simple circuit design, and good idle-tone performance are important. The major obstacle to overcome is the issue of stability. If the SNR is the major requirement, it will be a good choice. While the Multi-loop cascade has the advantages of low-order single-loop single-bit and high-order single-loop single-bit which are high SNR as well as the higher stability. But the multi-loop cascade has to near perfect matching between analog integrator and digital differentiator. It has high requirement in the switching-capacitor circuit. Therefore, Single-loop high-order designs is a good choice for the project.

Table 7 Comparison Between Single Loop And Multi-Loop Cascode

| Modulator type | Advantages | Disadvantages |
|---|---|---|
| Low-order single-loop single-bit ($\leq 3$) | • Guaranteed stability<br>• Simple loop filter design<br>• Simple circuit design | • Low SNR (except for high oversampling ratios)<br>• More prone to idling tones (dither may help) |
| High-order single-loop single-bit | • High SNR for modest oversampling ratios<br>• Simple circuit design<br>• Less prone to idling tones. | • Difficult loop filter design<br>• Stability is signal dependent<br>• Maximum input range must be restricted to ensure stability |
| Multi-loop cascade | • High SNR for modest oversampling ratios<br>• Stability guaranteed | • Requires near-perfect matching between analog integrator and digital differentiator. Complex switched-capacitor circuits are required to ensure matching.<br>• Imperfect matching may result in leakage of tones into baseband.<br>• Decimation filter must allow for must allow for multi-bit inputs. |

# V NOISE ANALYSIS AND BEHAVIOR MODEL

## 5.1 Noise analysis

After the compared the feedback with feed-forward as well as single loop and multi loop structure, we decided to use the feed-forward and single loop structure CRFB to achieve our target SNR=105dB. Where the oversampling ratio is 128 and the quantizer is 1.5bit. In upper part, the SNR performance of 2nd order single-loop is not enough to achieve the target even use 4 times OSR=256. Therefore, 3rd order modulation is the better choice.

Here it shows the performance in the ideal modulation, which has the quantization noise only, is pretty good as SNR=124.4dB. But in practice, there are many other noise in the circuit. The main non-idealities of the circuit which will be design in this project are following:

- Operational amplifier nonidealities:[28]
    1. Bandwidth of Op-amp;
    2. Slew rate of Op-amp;
    3. Operational amplifier saturation voltages.
- thermal noise(kT/C) of the Switch Capacitor structure;
- noise of op-amp;
- clock jitter at the input sampler;

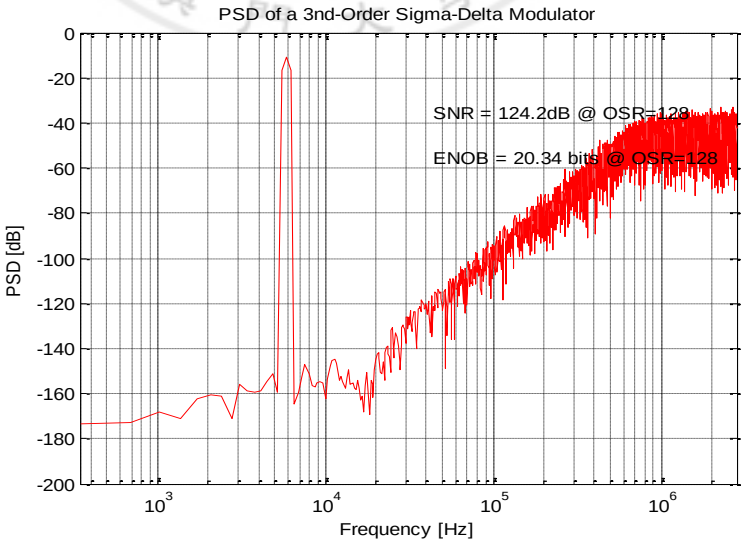



Figure 39 3rd order CRFB performance

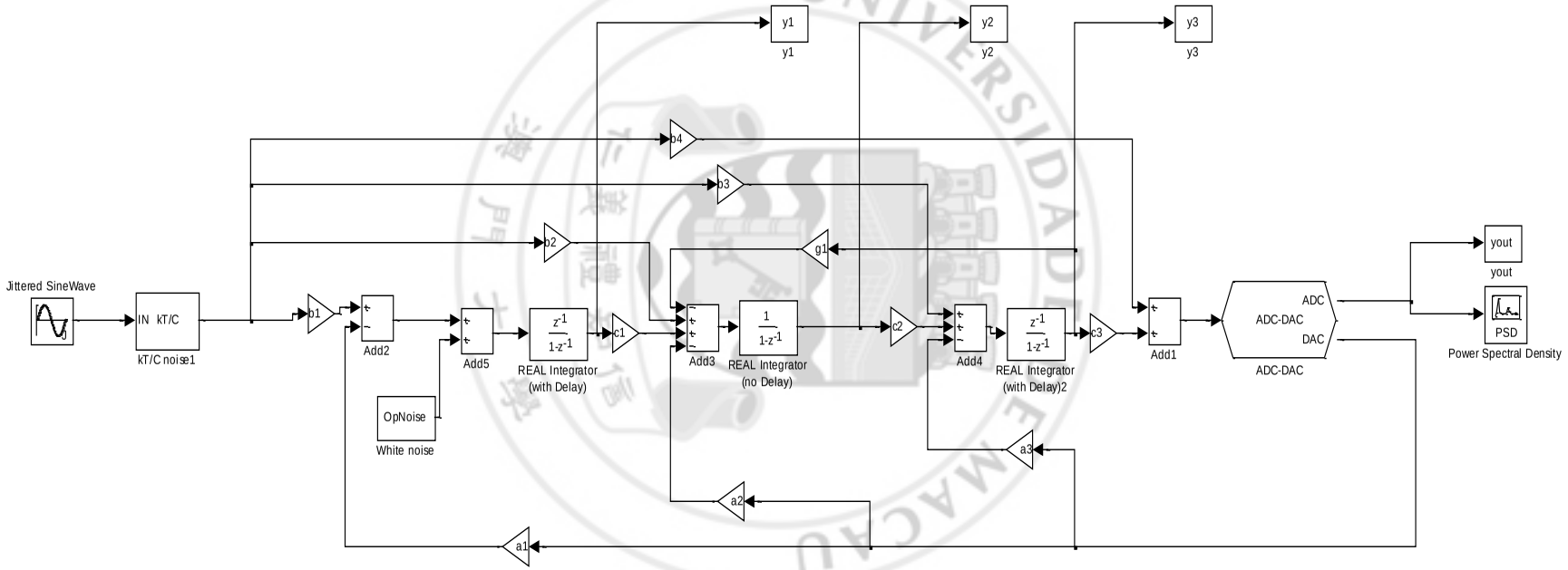



Figure 40 The 3rd order CRFB with the noise block

## A. Operational Amplifier Non-idealities

### a) Finite DC gain

The dc gain of the integrator in the figure of CRFF is closing to infinite, but in practice the DC gain can't be such high. If the dc gain cannot be infinite, the performance of the dc response of the integrator will decrease so that the total SNR performance will decrease as the dc gain decrease.[29]

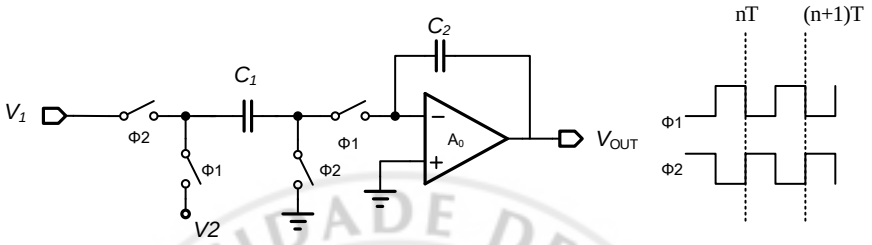



Figure 41 Switched capacitor integrator with finite gain op-amp

For ideal case which has infinite gain,

$$\frac{V_{out}}{V_1 - zV_2} = \left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1-z^{-1}} \tag{53}$$

It is a non-inverting integrator. And for the finite gain, the transform function become

$$\frac{V_{out}}{V_1 - zV_2} = \frac{C_1}{C_2}\left[\frac{A_0}{A_0+1+C_1/C_2}\right]\frac{z^{-1}}{1-\frac{(1+A_0)C_2}{C_1+C_2+A_0C_2}z^{-1}} \tag{54}$$

The pole shift from 1 to (1+A0)/ (1+A0+C1/C2). The shift of the pole causes the shift of the NTF zeroes because of the relationship between them. A second order modulator can be represented,

$$\text{NTF} \approx (1 - z_{p1}\cdot z^{-1})(1 - z_{p2}\cdot z^{-1}) \tag{55}$$

zp1 and zp2are the zeroes of the NTF cause by the shift.

In the situation that the A0 and capacitances are equal

$$\text{NTF} = (1 - z^{-1}\frac{A_0+1}{A_0+2})^2 \tag{56}$$

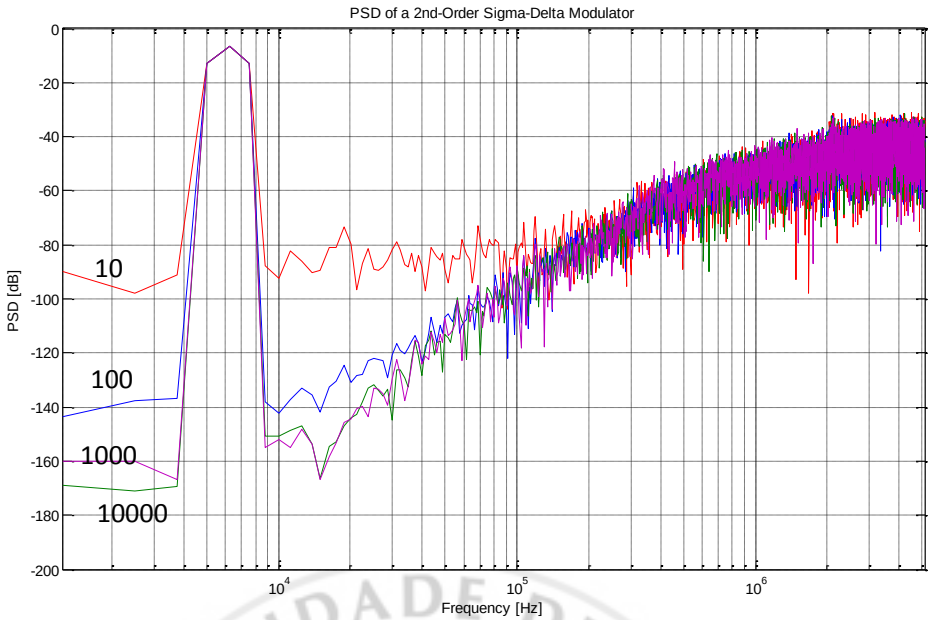



Figure 42 NTF of a second order modulator for three different dc gains of the op-amps.

It (fig 41) shows that only the shaping below a corner frequency fc will be affected by the finite dc gain. If the signal band is larger than fc, the noise power will not be affect by the change of the dc gain. And if the signal band is smaller than fc (fig 41), the noise power will increase as the dc gain of the op-amp decrease. Therefore, the finite dc gain is one of the non-idealitise which affects the SNR performance.

The fc (corner frequency) can be represented by

$$e^{S_p T} = \frac{A_0+1}{A_0+2} \tag{57}$$

$$f_c = \frac{f_s}{2\pi}\ln\{1-\frac{1}{A_0+2}\} \approx \frac{f_s}{2\pi(A_0+2)} \tag{58}$$

The SNR performance will not be affected if fB >> fc; therefore if the gain and oversampling ratio can satisfy π (A0+2)>>OSR, the SNR performance will be better. Therefore, we decrease the dc gain and see the performance of the whole system so that we can find a dc gain which is easy to achieve for the op-amp and dose not much affect the performance.

Table 8 The Performance Of System As Gain Decrease

| Finite DC gain | SNR |
|---|---|
| 80dB | 124.2dB |
| 60dB | 123.9dB |
| 54dB | 123.9dB |
| 52dB | 122.5dB |
| 50dB | 120.4dB |

It must be as it is shown that performance will be worse as DC gain decrease. And finally we choose the 54dB as the DC gain which is easy to achieve for the op-amp and dose not much affect the performance.

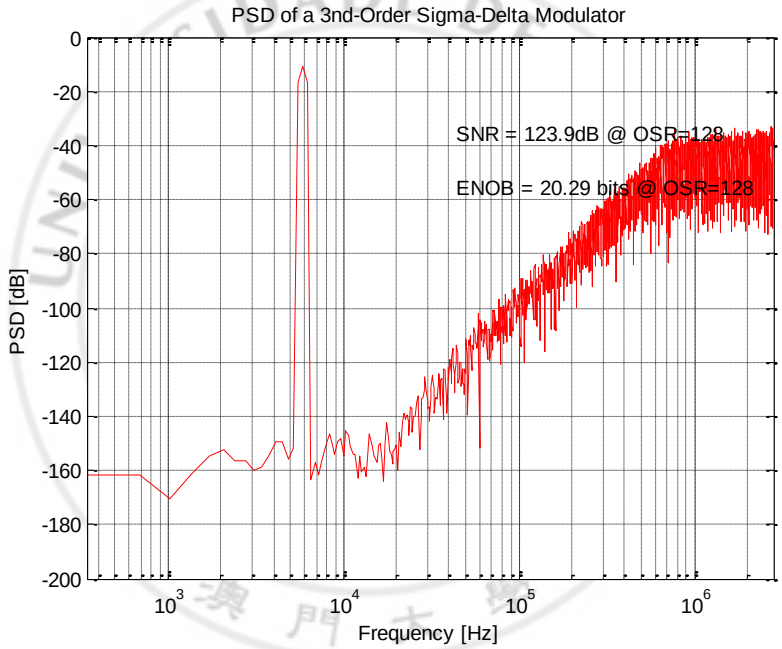



Figure 43 The system performance With 54dB gain

**b) Finite BW and SR**

The non-ideal integrator has finite bandwidth and slew rate which are the parameter in the matlab model of CRFF figure. The effect of the finite bandwidth and the finite slew rate are related to each other. Furthermore, they may be interpreted as a nonlinear gain. [28]

The finite op-amp bandwidth and slew-rate cause the settling error

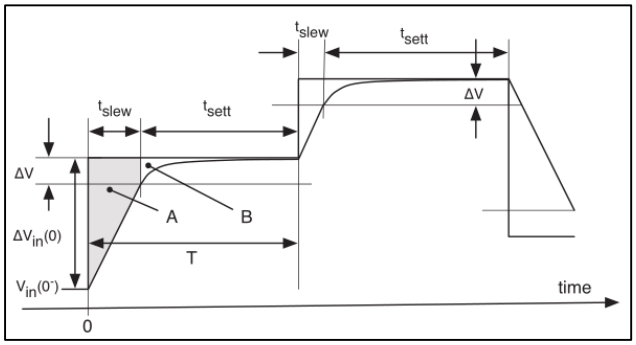



Figure 44 Response of a unity gain buffer with finite slew-rate and bandwidth

In Figure 44, it shows that since the integration phase only lasts Ts/2, for a certain bandwidth if the slew is such small that the signal cannot achieve the high point after half period. It causes an error. So, it the bandwidth is large enough the SR can set to be a small value. On the other hand, if the bandwidth is small, it requires a higher SR.

Also, we change the SR and BW to see the performance of the whole system so that we can find SR and BW which are easy to achieve for the op-amp and dose not much affect the performance.

The minimum value of the GBW is

$$\mathrm{GBW} = \mathrm{BW} * \mathrm{gain} = 22.05\mathrm{kHZ} * 500 = 11.025\mathrm{MHZ} \quad (59)$$

Table 9 The Performance Of System As Sr And Gbw Change

| GBW(MHz) | SR(V/us) | SNR(dB) |
|---|---|---|
| 12 | 100 | 124.2 |
| 12 | 90 | 118.8 |
| 12 | 80 | 112.8 |
| 20 | 80 | 123.3 |
| 30 | 80 | 123.9 |
| 40 | 80 | 124.2 |
| 40 | 70 | 124.2 |
| 40 | 60 | 124.2 |
| 40 | 50 | 124.2 |
| 40 | 40 | 124.2 |
| 40 | 30 | 121.8 |
| 50 | 30 | 124.2 |

Since, the higher GBW is easier to get than the higher SR we finally choose the GBW=50MHz and SR=30V/us to do the further error simulation and further design.

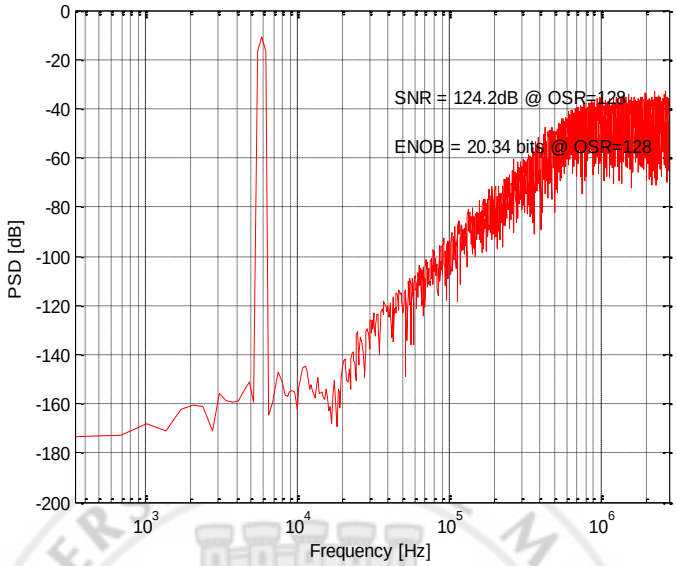



Figure 45 The system performance with GBW=50MHz and SR=30V/us

### c) Saturation voltages

As known, the when the signal excels saturation voltage of the op-amp the extra part of signal will be banned. For signal conversion, it will cause the distortion some part of the signal cannot be processed. Therefore the signal power decrease as well as the SNR performance decrease. In the model as shown in Fig CRFF, the saturation voltage is one of the parameter of the non-ideal integrator.

We decrease the saturation voltage to find the minimum value which doesn't cause distortion.

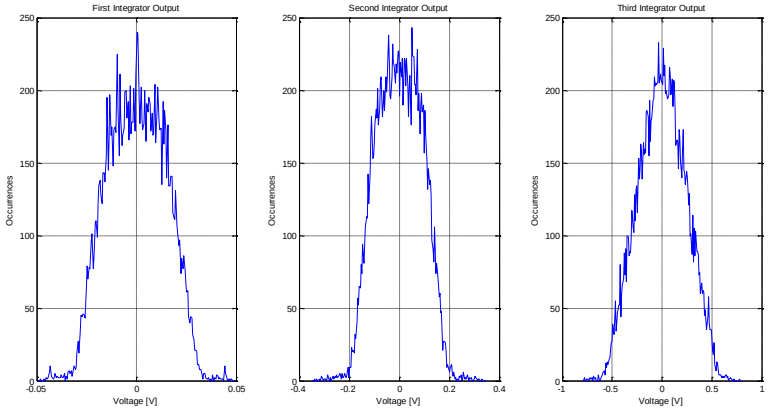



Figure 46 The output of each integrator with Input amplitude is ±0.5 V

Table 10 The Performance Of System As Saturation Voltage Change

| Saturation voltages(V) | SNR(dB) |
|---|---|
| ±3 | 124.2 |
| ±2.5 | 124.2 |
| ±2 | 124.2 |
| ±1 | 124.2 |
| ±0.8 | 120.3 |
| ±0.6 | 104.9 |

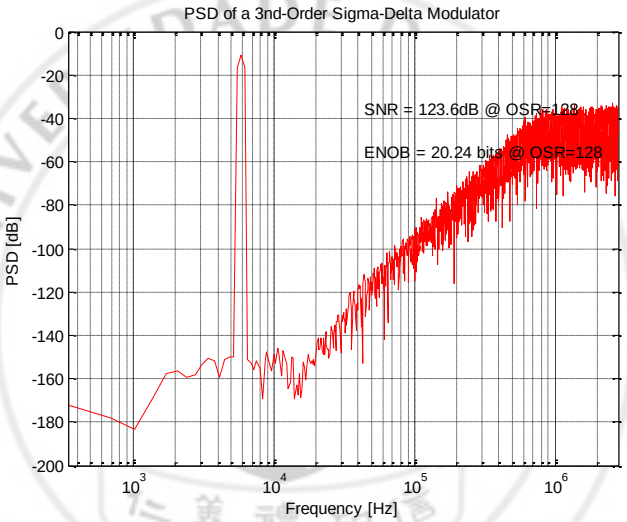



Figure 47 The system performance 1V saturation voltage

Here, we can see the saturation voltage of the op-amp should be larger than 1 V which is hard to achieve. So we will have some modification in the circuit design stage.

**B. Thermal and operation amplifier noise-Switches Thermal Noise (kT/C)**

In switch capacitor circuit, the random fluctuation of carriers due to thermal energy can cause the thermal noise which will be present even at equilibrium. Thermal noise has wide band and a white spectrum, it is only limited by the time constant of the switched capacitors or the bandwidth of the op-amp. The SC first-order $\Sigma\Delta$ modulator, as example, the sampling capacitor Cs is in series with a switch with finite resistance Ron. And periodically opens cause the sampling noise voltage onto Cs. The total thermal noise power can be represented by[28]

$$e_T{}^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_s)^2} df = \frac{kT}{C_s \cdot OSR} \quad (60)$$

Where k is the constant, T is the temperature in k,

From the table X, we can see the thermal noise is much larger than other noise. Therefore the switch thermal noise will dominate the other noise. And if the Cs is larger, the power consumption will be higher. Here, we choose Cs=1pF to do further analysis.

Table 11 The Performance Of System As Sampling Capacitance Change

| Switches Noise(Cs) | SNR(dB) |
|---|---|
| 2.5pF | 101.8 |
| 2pF | 99.9 |
| 1.5pF | 97.7 |
| 1pF | 96.6 |
| 0.5pF | 93.0 |

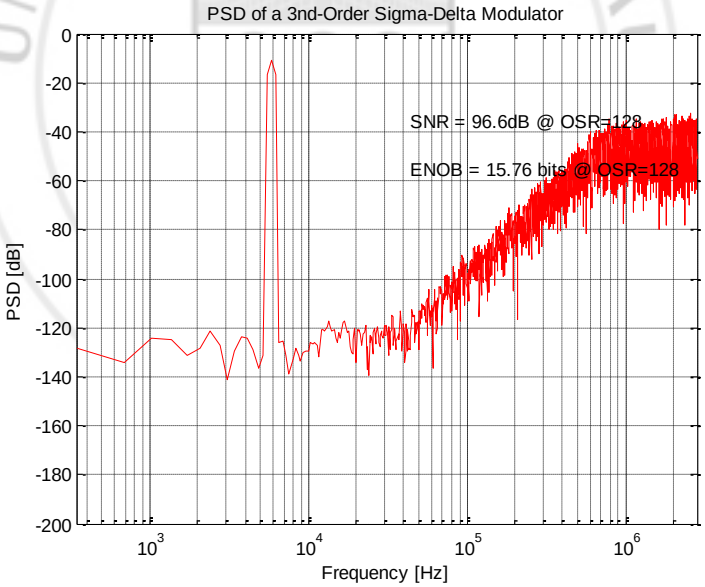



Figure 48 The system performance with Cs=1pF

### C. Operational Amplifier Noise

In this model we considered only thermal noise, while flicker (1/f) noise and dc offset are neglected. Through a transistor level noise simulation for the complete integrator in the proper clock phase which is including feedback, sampling and load capacitors, it evaluated the noise power $Vn^2$.

Table 12 Performance Of System As Input-Referred Operational Amplifier Noise Change

| Input-referred operational amplifier noise(Vn) | SNR(dB) |
|---|---|
| 50uVrms | 97.7 |
| 20uVrms | 105.7 |
| 10uVrms | 111.4 |
| 8.3uVrms | 112.8 |
| 5uVrms | 116.6 |

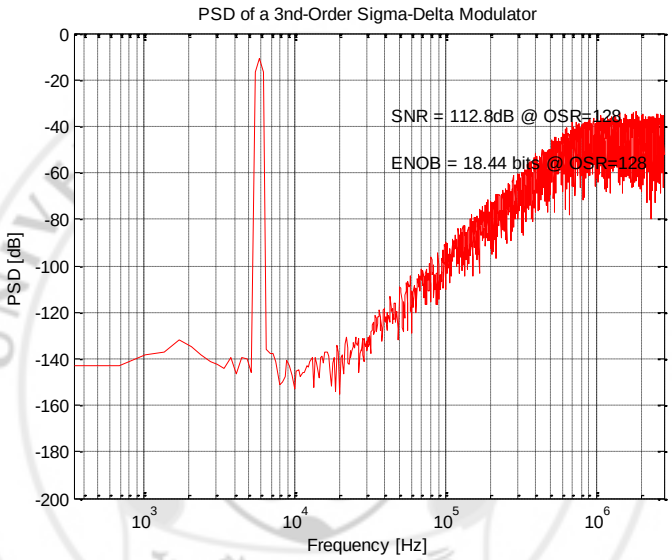



Figure 49 The system performance with Vn=8.3uV

The 8.3umV is calculated by some approximately method. We use 8.3uV [34] to do further simulation. But in practice, the operational amplifier noise will be larger.

### D. Clock Jitter

The operation of an SC circuit depends on complete charge transfers during each of the clock phases [39]. Once the analog signal has been sampled, the Switch-Capacitor circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the input sampling signal. This also means the structure and order of the $\Sigma\Delta$ modulator will not is not the factor of the

effect of the clock jitter on a sigma delta modulator.

For sampled system, the SNR limitations due to jitter can be determined by the following equation [9];

$$\text{SNR} = -20\log(2\pi f_{analog} t_{jitter}) \tag{61}$$

Where f is the analog input frequency, t is the jitter.

Therefore, given a frequency of operation and an SNR requirement, the clock jitter requirement can be determined as follows.

$$t_{jitter} = \frac{10^{\frac{-SNR}{20}}}{2\pi f_{analog}} = 34ps \tag{62}$$

SNR=124dB and input amplitude is 0.5V.

Table 13 The Performance Of System As Sampling Jitter Change

| Sampling Jitter($\Delta\tau$) | SNR(dB) |
|---|---|
| $34ps$ | 124.2 |
| $68ps$ | 124.2 |
| $100ps$ | 123.4 |
| $150ps$ | 122.5 |
| $200ps$ | 121.5 |
| $250ps$ | 120.7 |
| $300ps$ | 119.0 |

Nowadays, the $\Delta\tau = 34ps$ is a relax requirement.

**E. Overall noise**

Table 14 System Performance With Different Noise

| Sigma-delta Parameter | SNR(dB) |
|---|---|
| Ideal modulation | 124.2 |
| Finite DC gain | 123.9 |
| Finite | 124.2 |
| Finite Slew-rate | 124.2 |

| | |
|---|---|
| Saturation voltages | 123.6 |
| Sampling Jitter ($\Delta\boldsymbol{\tau}$ = | 124.2 |
| Switch (kT/C) noise | 96.6 |
| Input-referred operational | 112.8 |
| Including all of the non- | 95-96.5 |

As the table above, all of the noise are considered. And the final result is a range because of the random noise in the model.

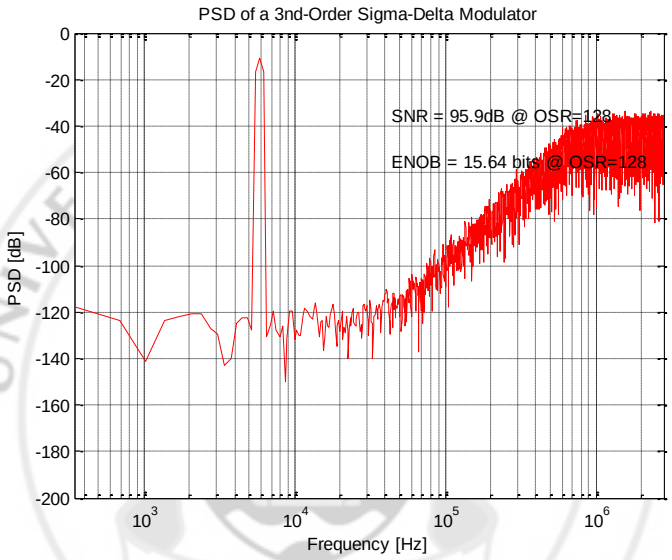



Figure 50 The system performance

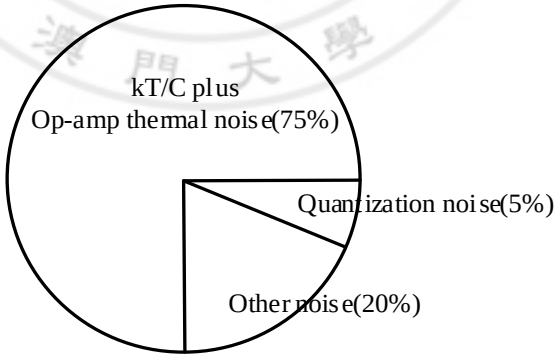



Figure 51 Noise budget

In this part, the noise budget of the system is shown (fig 48). The kT/C and op-amp thermal noise are effecting the performance of the system mostly while the quantization noise just effect the performance a little bit. Therefore, the decrease the kT/C and op-amp thermal noise will be the key work to increase the SNR performance of the system.

Moreover the preliminary design doesn't achieve the target, the further decision can be made.

## 5.2 Behavioral model

According to the analysis and comparison result, the further decision is using CRFB structure with OSR=256 and 1.5bit quantizer. Moreover, repeating the analysis above can get the behavior model of the system

Table 15 Behavior Model Of The Project

| Sigma-delta Parameter | SNR(dB) |
|---|---|
| **Ideal modulation** | 134.8 |
| **Finite DC gain (G=58dB, 58dB, 50dB)** | 130.6 |
| **Finite bandwidth(GBW=100MHz)** | 134.8 |
| **Finite Slew-rate (SR=60V/us)** | 134.8 |
| **Saturation voltages (\|Vmax\|=1V)** | 134.8 |
| **Sampling Jitter ($\Delta\tau = 17ps$)** | 130.7 |
| **Switch (kT/C) noise (Cs=10pF)** | 110.4 |
| **Input-referred operational amplifier noise (Vn=1.5uV)** | 108 |
| **Including all of the non-idealities** | 107-107.5 |

The swing is acceptable for the output of integrator. Moreover, the SNR performance can achieve the setting target SNR=105dB.

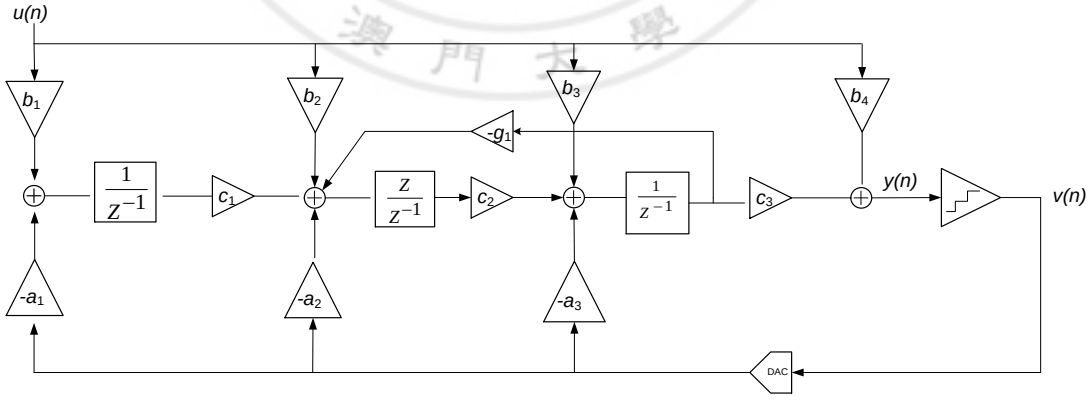



Figure 52 3rd order CRFB architecture

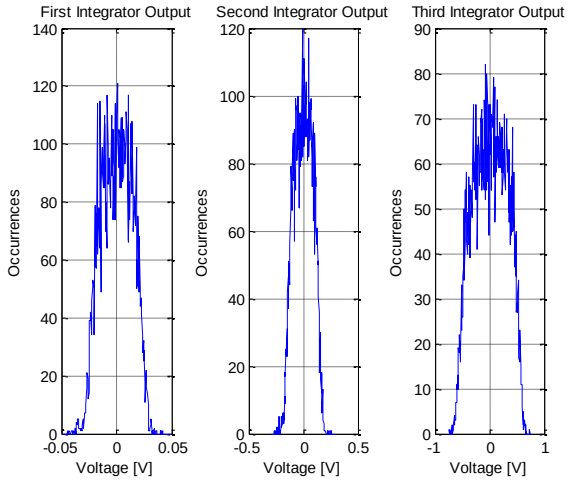



Figure 53 The output swing of each integrator with Input amplitude is ±0.4 V

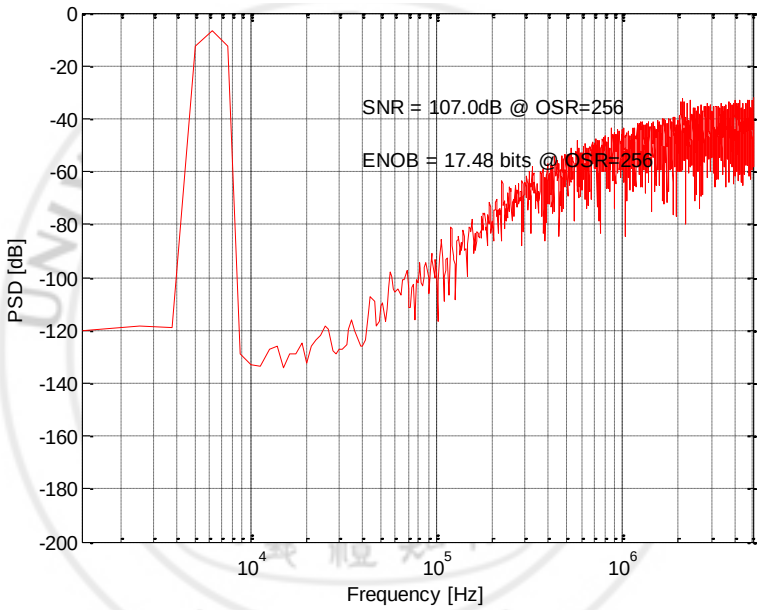



Figure 54 the system performance

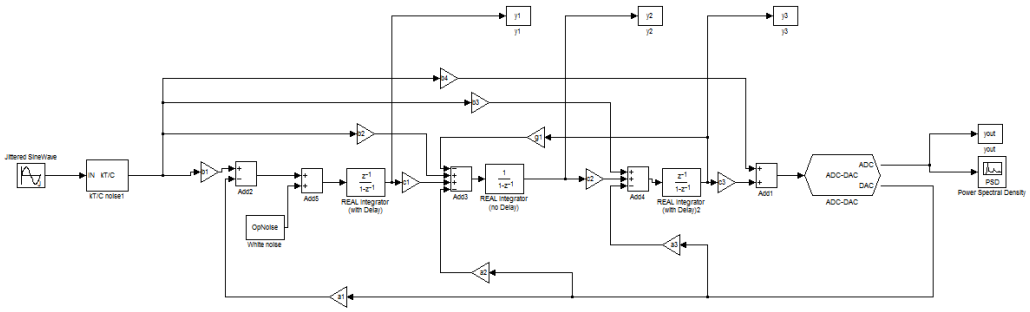


Figure 55 The 3rd order CRFB with noise block in matlab

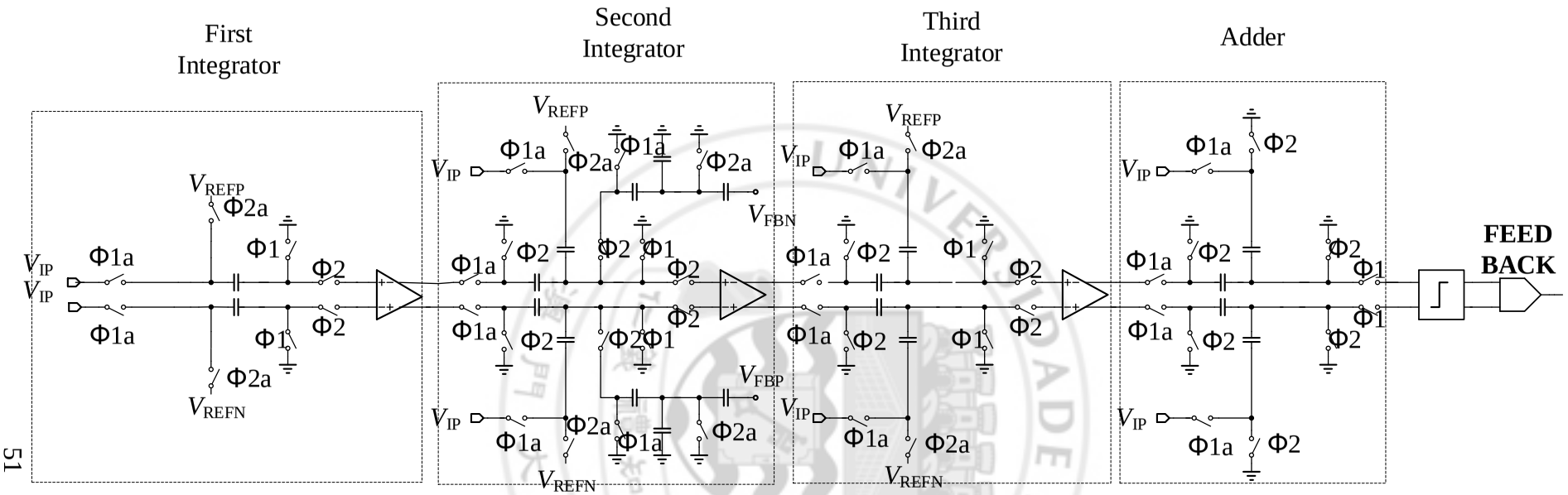



Figure 56 The conventional CRFB circuit system

# VI CIRCUIT DESIGN

For the system, it mainly include clock generator, adder, quantizer and three integrators. In this project, special integrator called Charge-Pump integrator is used as the first integrator which is the most power hungry one.

## 6.1 Charge Pump Integrator

As upper mention, in order to get high resolution system, large OSR and large sampling capacitor are require to reduce the thermal noise which constraints the power consumption of op-amp. Moreover, one of the main constraints of the chosen structure CRFB is the high requirement of first op-amp which requires high DC gain as well as high power consumption. In this project, a special integrator called charge-pump integrator shown in above figure is used to improve the power efficiency.[30]

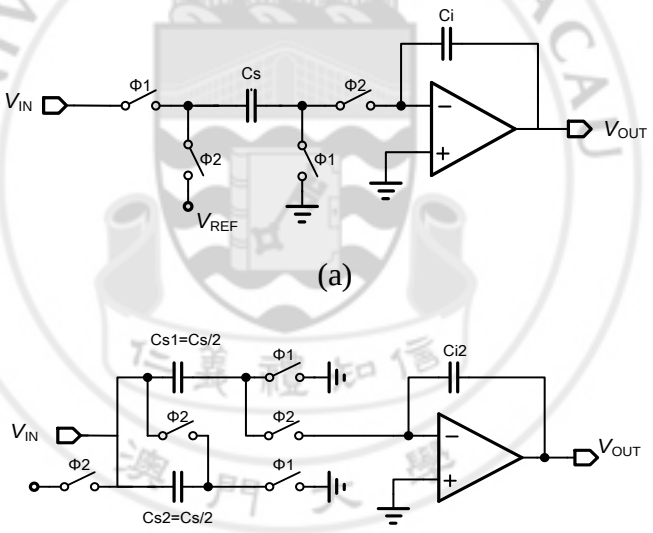



Figure 57 (a) Conventional Switch capacitor integrator and (b) charge pump integrator

The figure above (a) shows the normal SC (switch capacitor) integrator. During $\Phi_1$, the input signal is sampling into the sampling capacitor Cs. During $\Phi_2$, the sampling capacitor Cs will connect to the virtual ground and reference voltage feedback from the DAC to integrate (Vin – Vref). At that time the charge sampled in the sampling capacitor in $\Phi_1$ will transform into Ci. For charge pump integrator shown in fig (b), during sampling phase $\Phi_1$, two sampling capacitor Cs1=Cs2=Cs/2 with sample the input signal

same as the conventional one, during $\Phi_2$, this two sampling capacitor will connect together between the virtual ground and the reference voltage feedback from the DAC. As figure (c) and (d) shown, during $\Phi_2$ the sampling capacitor will become Cs/4, but the signal in it is double, therefore it needs a double of reference voltage to integrate $2(V_{in}-V_{ref})$ by using Ci2=Ci/2.

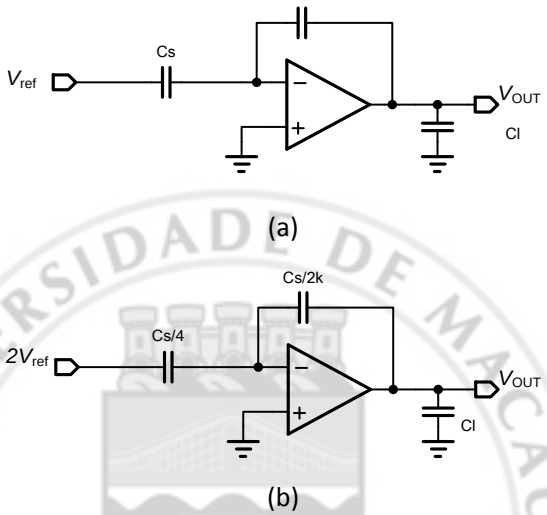



Figure 58 (c) Conventional Switch capacitor integrator and (d) charge pump integrator during Φ2(integration phase)

**Power Consumption of Charge Pump Integrator**

For a typical op-amp, the $g_m$ (transconductance) of the input differential pair is proportional to the power of the whole op-amp.

$$POW_{OP} \propto g_m \tag{63}$$

The transconductance of the op-amp with sampling rate and settling time required is given by [30]

$$g_m = \frac{\omega_{-3dB} C_L}{\beta} \tag{64}$$

Where $\omega_{-3dB}\, is$ the -3dB frequency, β is is the feedback factor the $C_L$ is the capacitance loading.

From figure (c) and (d) ignore the parasitic capacitor, the $C_L$ and β for normal integrator is given by

$$C_L = \frac{C_s}{k+1} + C_l \tag{65}$$

$$\beta = \frac{1}{k+1} \tag{66}$$

For the CP integrator

$$C_L{}' = \frac{C_s/2}{k+2} + C_l \tag{67}$$

$$\beta' = \frac{2}{k+2} \tag{68}$$

The effective closed-loop load capacitance $C_L/\beta$ of both situation is given by

$$\frac{C_L}{\beta} = C_s + C_l(k+1) \tag{69}$$

$$(\frac{C_L}{\beta})' = \frac{C_s}{4} + C_l(\frac{k}{2} + 1) \tag{70}$$

Generally, k is smaller than 1 and Cs>Cl. Therefore $\left(\frac{C_L}{\beta}\right)' \approx \frac{C_L}{4\beta}$, the thermal noise analysis shows CP integrator has same input-referred thermal noise as the normal one [30]. In the sampling phase, the thermal noise of CP integrator and conventional integrator are the same. During $\Phi_2$, since the connection of Cs1 and Cs2, the sample noise of the CP integrator will be four times of conventional one. But in this period the signal in the Cs1 and Cs2 is double of the input as well as the reference voltage. Hence, in the same requirement of settling time, thermal noise performance as well as the sampling rate for this two kind of integrator:

$$g_m' = \frac{g_m}{4} \tag{71}$$

Which will correspond to the reduction of the power consumption by about four time.

$$POW_{op}' = \frac{POW_{OP}}{4} \tag{72}$$

As a conclusion, charge pump integrator is a good choice for this project.

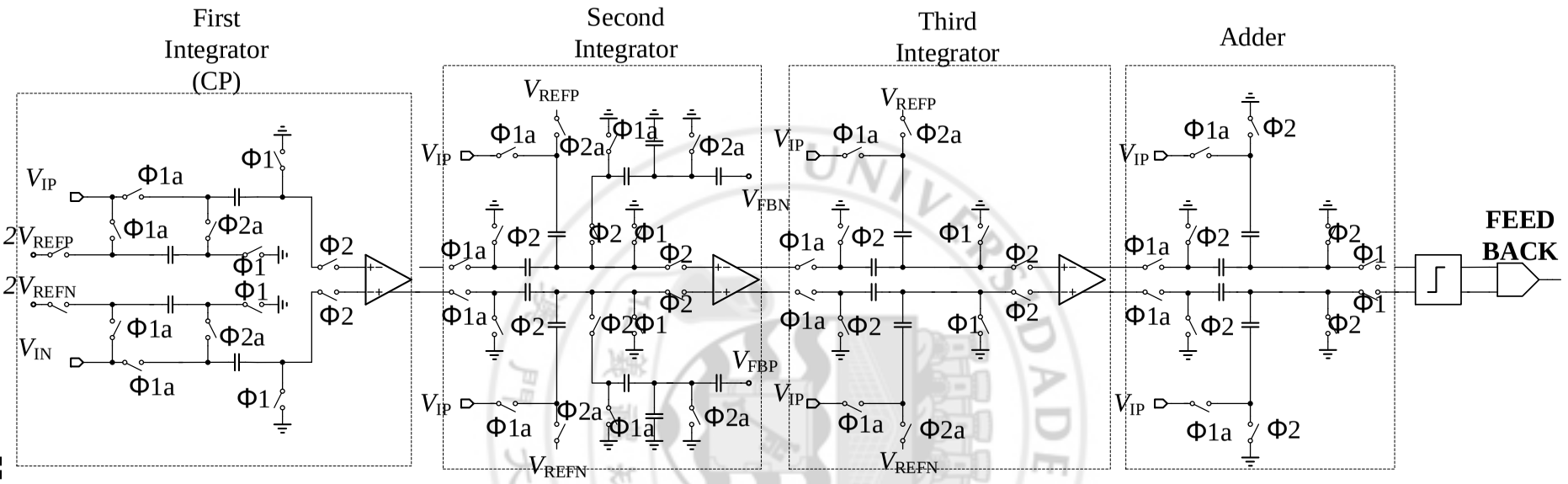



Figure 59 The CRFB circuit system with CP integrator

## 6.2 Op-Amp Design

For a normal sigma delta ADC with a large OSR, the first order loop will dominates no matter the performance as well as the power consumption. The power of the first Op-amp depends on the thermal noise, sampling rate and settling time. Therefore the first integrator is one of the key parts in the system. Repeat the procedure to find the new requirement of the first op-amp. For the normal simulation in matlab, the requirement gain of the first op-amp is 58dB

Table 16 New Gian Requirement Of First Op-Amp

| **The gain of first Op-amp(dB)** | **simulation result of Cadence(dB)** |
|---|---|
| 54 | 133 |
| 50 | 133 |
| 48 | 133 |
| 46 | 132 |
| 42 | 130 |

Using the new technique, the require gain of the first integrator is reduce from 58dB to 48dB almost 4 times reduction.

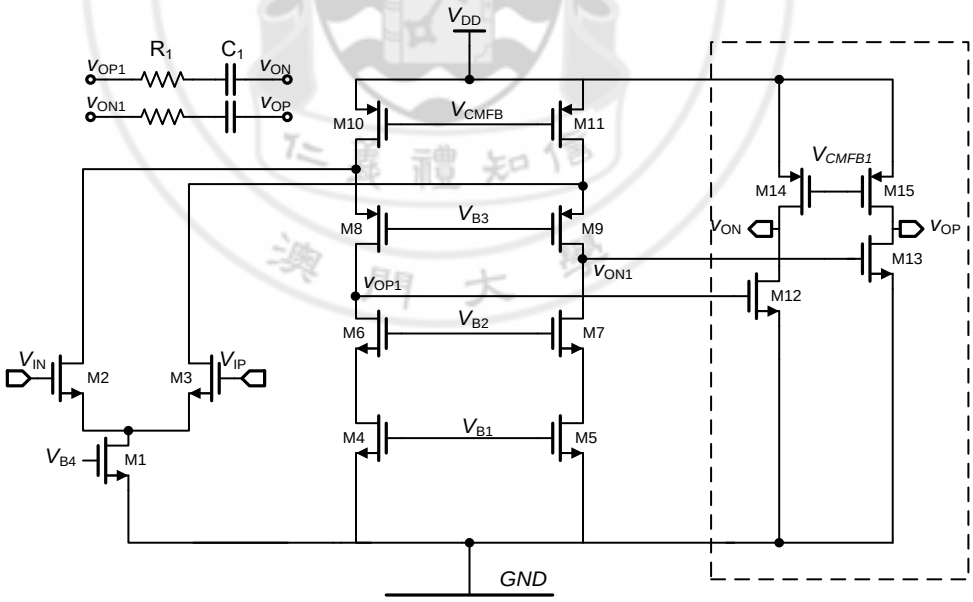



Figure 60 First op-amp structure

In order to fulfill the requirement of the first op-amp especial gain, GBW, SR and the swing, 2 stage op-amp using folded-cascode is chosen. Using folded-cascode with as first stage can get a high gain, and the common source amplifier can give the remaining gain and large output swing for the op-amp. And since the reference voltage of the CP

integrator is double, the input deferential pair of the op-amp must be NMOS. If here using PMOS, the input differential pair can't be saturated. To implement GBW and phase margin requirement, miller compensation is needed.

For the miller compensation,

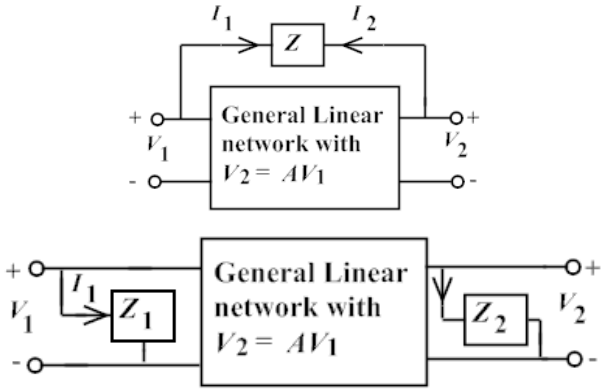



Figure 61 The feedback test circuit

$$Z_1 = \frac{Z_F}{1-A} \; and \; Z_2 = \frac{Z_F}{1-\frac{1}{A}}$$

For capacitor,

$$C_1 = C(1+A) \; and \; C_2 = C\left(1+\frac{1}{A}\right) \tag{73}$$

Where A is negative number. Therefore, a smaller capacitor is used to compensate the amplifier. And here $C_C$ is the miller capacitor which is used to separate the main pole and the side poles that one of the poles is leading to other that can decrease the GBW. Moreover, the R is a nulling resistor which can let the zeros at the right plane move to left plane thus the phase margin will be stable and increase.

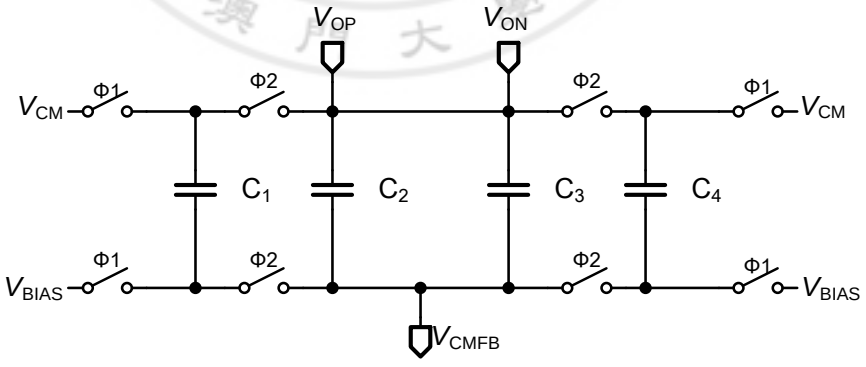



Figure 62 The common mode feedback structure

In order to stabilize the output common mode voltage, the switch- capacitor common mode feedback circuit is used. In general, a common mode feedback circuit consists of a common detect circuit and a comparison amplifier.[14] The difference between output

voltage of the CMFB circuit and the output of the op-amp is similar to the difference between Vbias and Vcm.

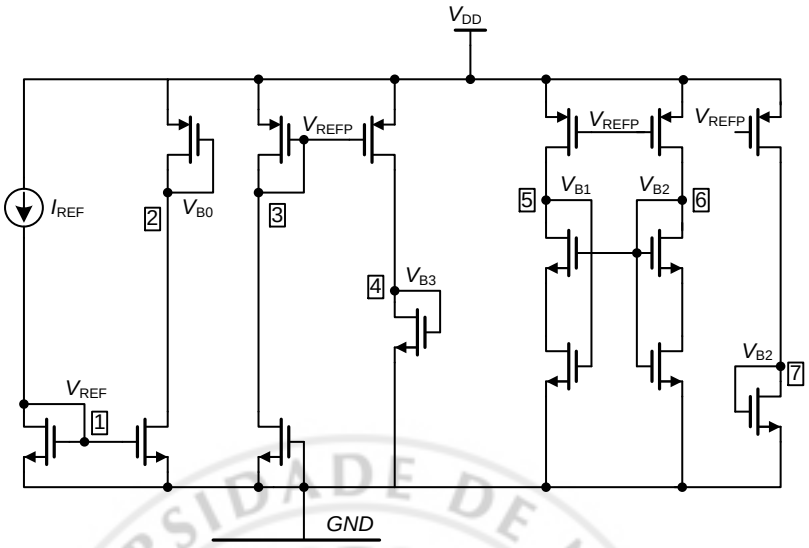



Figure 63 The baising circuit

Build the biasing circuit basic on the current mirror theorem.[35]

Table 17 1st op-amp performance

| | Requirement | 1st op-amp |
|---|---|---|
| Gain | 48dB | 58dB |
| GBW(Hz) | 100M | 231M |
| SR(V/us) | 60 | 120 |

For second op-amp, the requirement is more relax than the first one except the gain. Here a 1 stage folded-cascode with gain boosting [10] is used. Since the PMOS differential pair for folded-cascode architecture allows low common voltage, in second order the input common voltage is 500mV. Besides, the PMOS input pair can supply a large overdrive voltage which can relaxes the design of the switch.

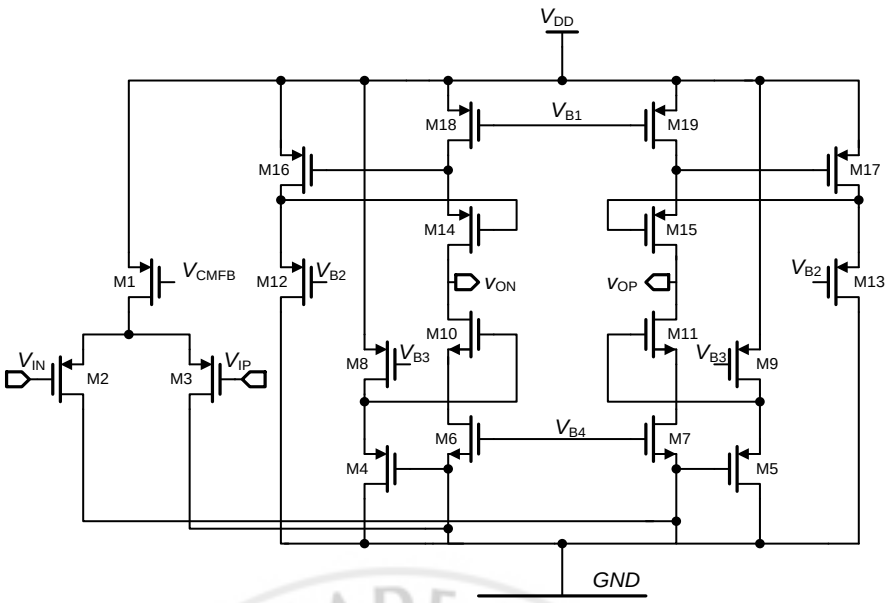



Figure 64 Second op-amp structure

Table 18 2nd Op-Amp Performance

| | Requirement | 1st op-amp |
|---|---|---|
| Gain | 58dB | 62dB |
| GBW(Hz) | 100M | 332M |
| SR(V/us) | 60 | 115 |

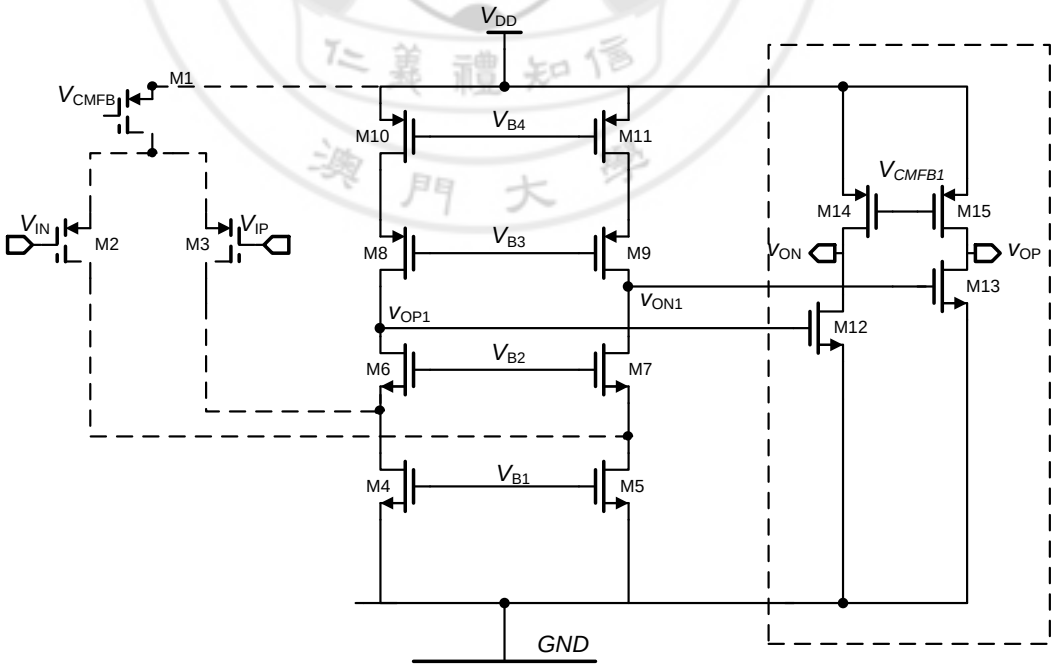



Figure 65 Second op-amp structure

Table 19 3rd Op-Amp Performance

| | Requirement | 1st op-amp |
|---|---|---|
| Gain | 50dB | 51dB |
| GBW(Hz) | 100M | 187M |
| SR(V/us) | 60 | 110 |

For third integrator, the output swing is as large as $\pm 300\text{mV}$, it is hard to build 1 stage op-amp with $\pm 300\text{mV}$ swing to get a high gain when full scare is 1V. Therefore, 2 stage architecture is needed.

## 6.3 Zero Optimization

For the CRFB structure, it needs a local feedback from third integrator output to second integrator input to make up a resonator which effects the zero. However, the local feedback coefficient is very small generally. For example, in this project this local feedback coefficient is g=-9.03*10^-5 corresponding to a Cb=9a, it need a very small capacitor which is impractical small to implement this coefficient.

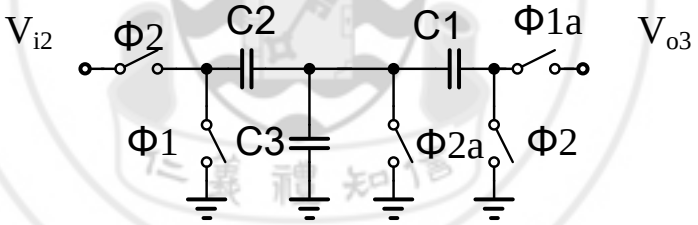



Figure 66 The SC local feedback

Therefore, a switch capacitor circuit [47] shown above figure 64 is used to implement the local feedback instead of a single capacitor in this project.

During $\Phi_1$, C1, C2 and C3 will sample the signal from V3. But only the charge in C2 is transform to the second integrator in $\Phi_2$. According to that, a series suitable capacitor can replace the impractical small capacitor. It needs charge in C2 is same as the Cb.

$$Q = g \cdot V_{o3}$$

The charge in C2 and C3 is given by

$$Q_2 = V_{o3} \frac{C_1 || (C_2 + C_3)}{2} \cdot \frac{C_2}{C_3 + C_2} \tag{74}$$

$$Q_2 = Q$$

Set up two of them, can get the other one.

## 6.4 1.5 bit quantizer

The 3-level-quantizer can be implemented from the simple comparator.

The Figure 67 Comparator schematic diagram shows the comparator schematic [12]. The dimension of the transistors we used is small, actually because of the bandwidth and speed's low requirement. It includes two input transistors (M2, M3), and one clock transistor (M1).

The comparator works differently during two phases, when the CLK fails, precharge transistors M8 and M9 (also M10 and M11) are turning on, so the outputs of comparator are reset to Vdd. In another phase, when CLK starts to rise, the tail current (M1) of the differential pair is turned on, the voltage at output nodes fails with a fast rate, and the voltage imbalance is created.

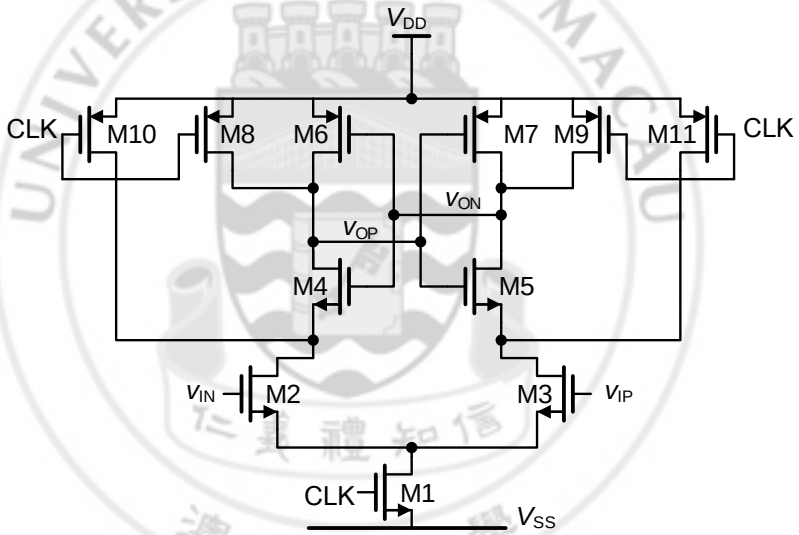



Figure 67 Comparator schematic diagram

In the system, for the reason of eliminate the comparator kickback, the comparator regenerates between Φ1 and Φ2, so the settling transients are not disturbed. Furthermore, an RS flip-flop can be used to keep the output during the hold period.

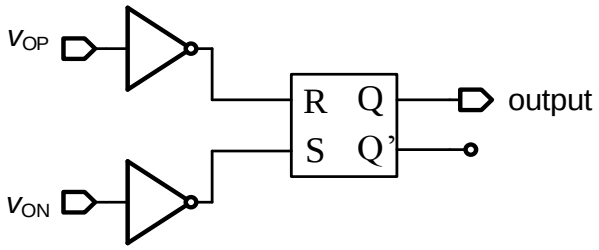



Figure 68 RS flip-flop

By checking the truth table of SR-latch in Table 20. If $\overline{\text{Vop}}$ is applied to R, and $\overline{\text{Von}}$

is applied to S, the condition is perfectly matched, and the output can be hold without any other disturbance.

Table 20 Comparison Of SR-Latch And Comparator

| SR latch operation | | | | Comparator | | | |
|---|---|---|---|---|---|---|---|
| Characteristic table | | | | Characteristic table | | | |
| **S** | **R** | **Q next** | **Action** | **Vop** | **Von** | **output** | **action** |
| 0 | 0 | Q | Hold state | 0 | 0 | X | Not allowed |
| 0 | 1 | 0 | reset | 0 | 1 | 0 | reset |
| 1 | 0 | 1 | set | 1 | 0 | 1 | set |
| 1 | 1 | X | Not allowed | 1 | 1 | 1 | Hold state |

In this system, a 1.5bit quantizer is used to get a higher SNDR. The circuit of the circuit is shown in Figure 69 . Two comparators are used to generate two digits, here D0 indicates the higher digit and D1 indicates the lower digit.

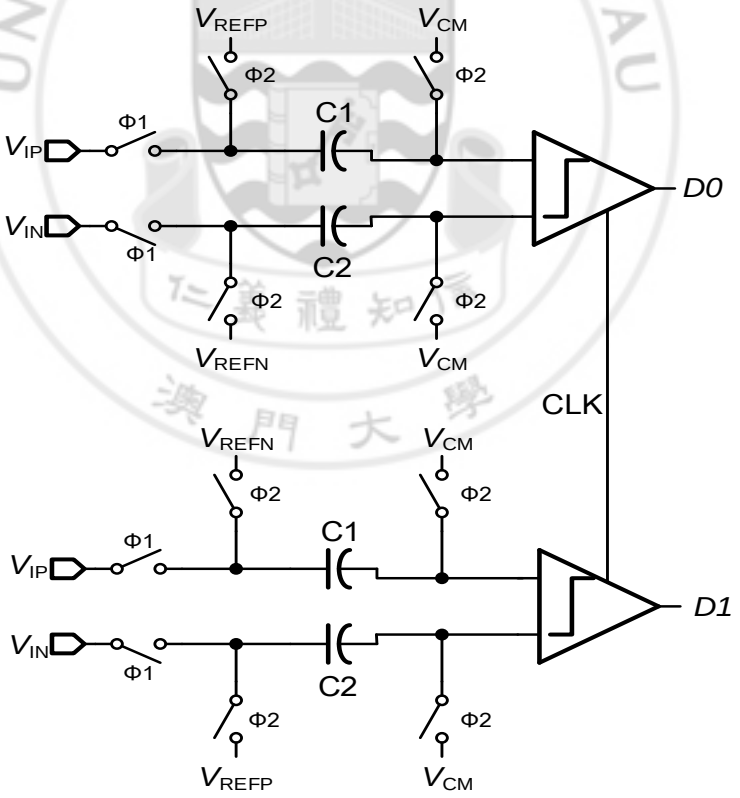



Figure 69 3-level-quantizer schematic

The switched-capacitor architecture is to make the comparison between the input voltage and the two reference voltages. For the Vcm=500mV, and also considering the swing of the input voltage, the reference voltages are set as Vrefp=600mV and

Vrefn=400mV.

## 6.5 Clock Generator

As we known, a number of clock phases that are obtained from a master clock. For example, the delay, overlapping or non-overlapping specific features are needed for our design.

The figure below shows a structure which generates four scheduled phases from one preliminary phase, mainly controlled by the cross-coupled flip-flop, [38]

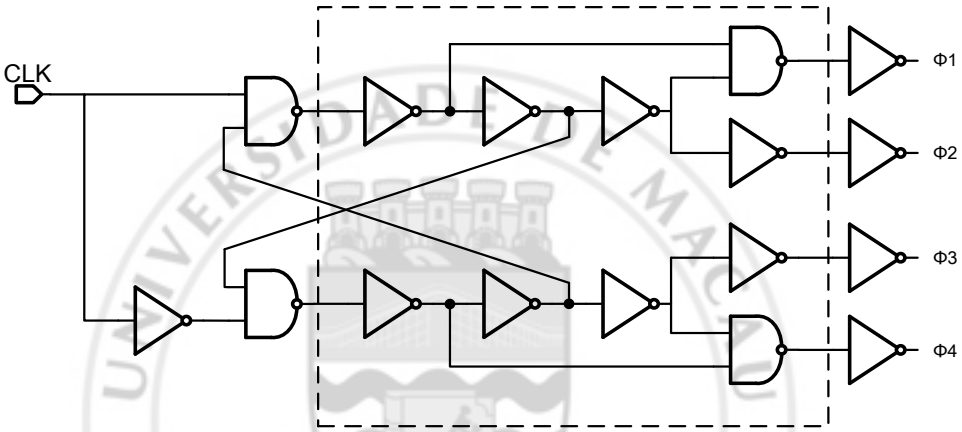



Figure 70 The clock generation logic

In that Figure 70, all the logic gates in the square frame are settled as 1ns delay, when the input phase goes from 1 to 0, for Φ2, there is a delay of four inverters after the input phase. For Φ1, observing that one input of output NAND gate is from the output of first inverter, following this, it'll decreases after 2 delay time. So the falling edge of Φ1 is 2-delay-time before the Φ2. Following this, Φ3 and Φ4 are also transformed into non-overlapping phases at the output nodes.

For the first input clock, the period is calculated from the system's requirement. The bandwidth is 20 kHz, and the OSR is 256, so the sampling frequency is 2*bandwidth*OSR= 10.24e6 Hz.

## 6.6 Feedback Logic

The feedback signal can also be implemented by logic gates, the 1.5 bit quantizer gives

the output signal D0 and D1, here D0 indicates the higher digit and D1 indicates the lower digit. The feedback controls the transfer of data, so that the analog architecture is configured.

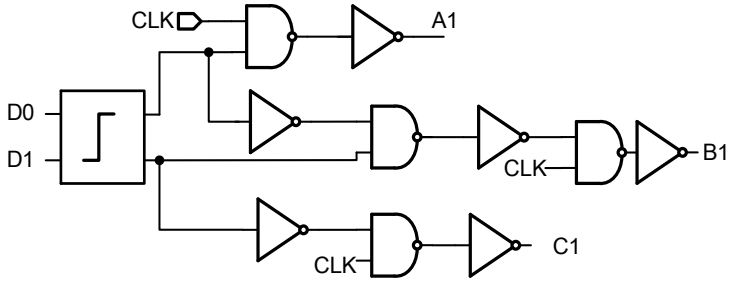



Figure 71 The feedback circuit

Referring to the system, it has three different feedback voltages, Vdd is given to A1, and also Vcm defined as B1, Vgnd as C1. Noticing all the three outputs are connected with an NAND gate which has a 'CLK' input, the feedback logic only works when the working phase equals to one during the hold period. The truth table is:

Table 21 The Feedback Logic

| | A1 | B1 | C1 |
|---|---|---|---|
| D0=0; D1=0 | 1 | 0 | 0 |
| D0=0; D1=1 | 0 | 1 | 0 |
| D0=1; D1=0 | 1 | 0 | 1 |
| D0=1; D1=1 | 0 | 0 | 1 |

The Table 21 shows that when output is low (D0=0; D1=1), the feedback voltage is high (A1=Vdd). In opposite, when output is high (D0=1; D1=1), the feedback voltage is low (C1=Vgnd). When' D0=0; D1=1', the output is connected with B1=Vcm.

As a reminder, here 'D0=1; D1=0' is not possible as D0 and D1 are from the 3-level-quantizer output.

## 6.7 Switches Replacing

For discrete-time sigma-delta ADC, the sample and hold circuit is typically used at the front of each stage. With the requirement of high speed and linearity, sampling switch

should maintain the ability of transfer the signals precisely. Also for different parts in the ADC, unlike types of switches are needed.[35]

- **MOSFET Switch**

So from figure it is a simple sampling circuit, it includes a switch and a capacitor.it works because (a) when passing current is zero, the switch can also be turned on. (b) When turning on, no matter how the voltage of bulk changes, it doesn't affect the voltage of drain and source.

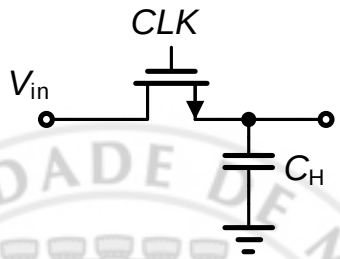



Figure 72 MOSFET as a switch

From the simulation, the switch is bidirectional. So when CLK goes high, the circuit can track the input signal, and if CLK goes low, the capacitor can hold the signal until the next period.

- **CMOS Switch**

CMOS switch can also be called transmission gate. It is often used when very large or small voltage input, under such situation, the transmission resistor will change critically, and will cause certain distortion. [35]

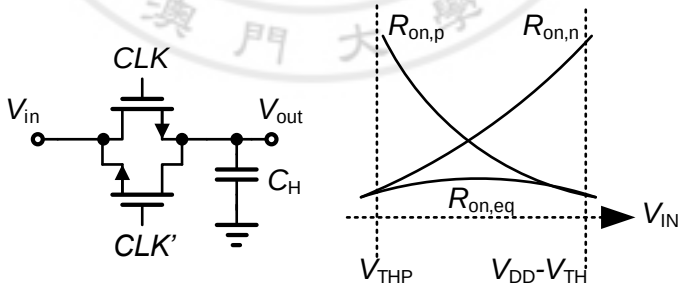



Figure 73 The transmission gate

So why it is reasonable to use switch when the rail-to-rail voltage transferred, the shows that the equivalent resistant is much stable than the single transistor switch. Moreover, to avoid uncertainty of the sampling, NMOS and PMOS switch should turn on or off at the same time

- **Bootstrapped Switch**

Our design uses low supply voltage (1V), some non-linearity may occur when the rail-to-rail input voltage enters at the first stage. To obtain constant conductance, the bootstrap technique can be used to keep the gate-source voltage at a certain value which is independent of the input signals.

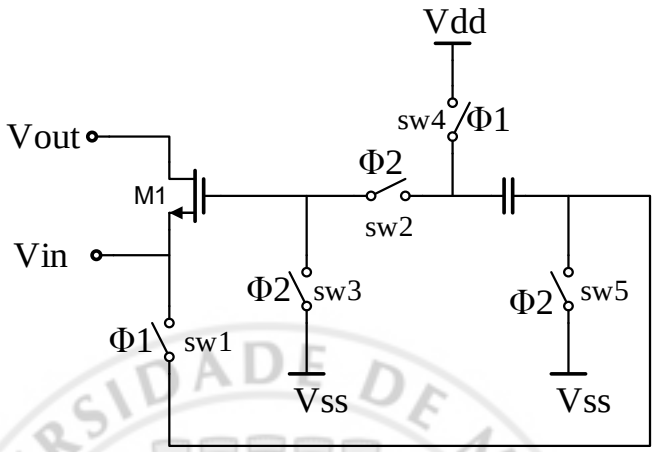



Figure 74 Fundamental principle of bootstrapped switch [37]

The Figure 74 shows the basic structure, Φ1 and Φ2 are two non-overlapping phases in the ADC. During Φ2 which is the hold period, the transistor's gates connects to Vss through switch2, the whole bootstrapped switch is in 'off' state, at the same time, the capacitor is charged to Vdd through switch4 and switch 5 until the next period.

During Φ1, switch 1 and switch 2 are closed, so the gate-source voltage of M1 is equal to the voltage of the charged capacitor, which means Vdd.

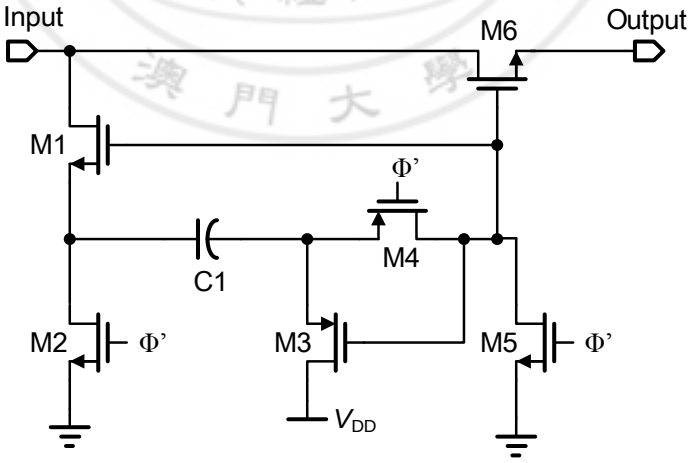



Figure 75 Bootstrapped Switch

The figure shows a simple bootstrapped switch following the basic principle, when Φ=0, C1 is charged through M2 and M3, and M6's gate is connected to zero, when Φ=1, the gate voltage of M4 equals input signal plus VDD through M1 and M4. For the capacitor,

it should not too large because we need a fast rate to store and release the charge, we set it as 300f F.

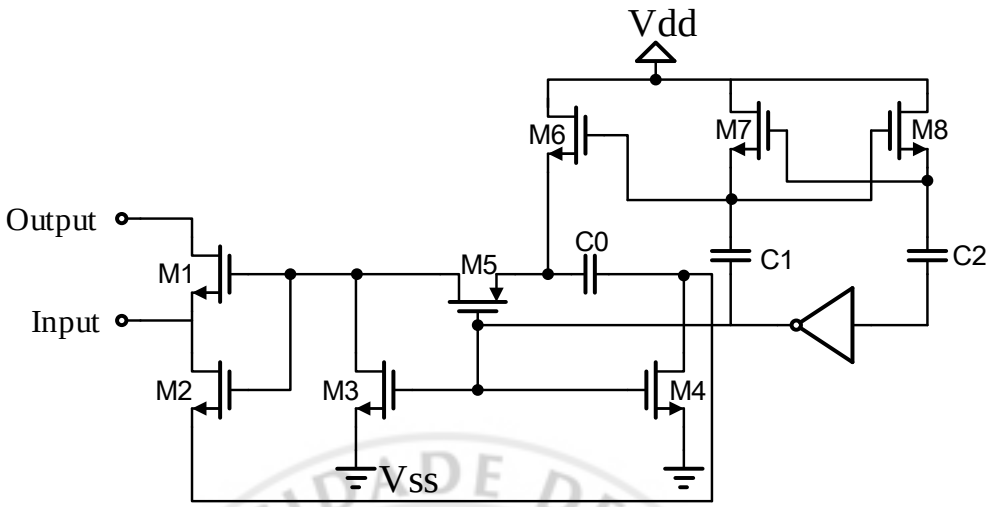



Figure 76 Bootstrapped switch with implementation

During the simulation, it is still found that the simple bootstrapped switch still cannot fulfill the target performance, for Figure 76, an implemented switch is introduced.

The improvement focus on the M2 and M6, as we can see, M2 functions as an input switch, which is also bootstrapped.

For M6, because the switch4 may leak when the bootstrap capacitor is charged to a voltage level exceeding Vdd. Differ from the formal case, the switch4, a NMOS is used to replace the PMOS switch. Plus, a charge-pump voltage shifter is built by M7, M8, C1, C2, so a clock level between Vdd to 2Vdd can be used to control the NMOS M6.

As a supplement, for switch distortion analysis [16], we know the one main part from the Charge injection. However, because we use bootstrap, Vgs is a constant value, so the error voltage is signal independent, also for the reason of differential input, this error will be finally be cancelled. For the Clock feed-through problem, its value also doesn't affect the final performance. Actually the main noise comes from the thermal noise, so in this report we won’t talk in details.

# VII PERFORMANCE

The output waveform as well as the PSD for the 3 order CRFB sigma delta analog to digital converter with charge pump integrator is shown below. It clearly shows the input

signal and the noise most of which is shifted to the high frequency band (>20kHz) that will be filter by a low-pass filter. And the in-band (<20kHz) noise level is very low about -110dB. A zero locates at about 15kHz. The total Signal-to-Noise-Distortion Ratio is 106dB. The digital signal output is shown in figure 78. Moreover, Figure 79 the gives the SNDR performance versus different input amplitude. The corresponding dynamic range is 107dB.

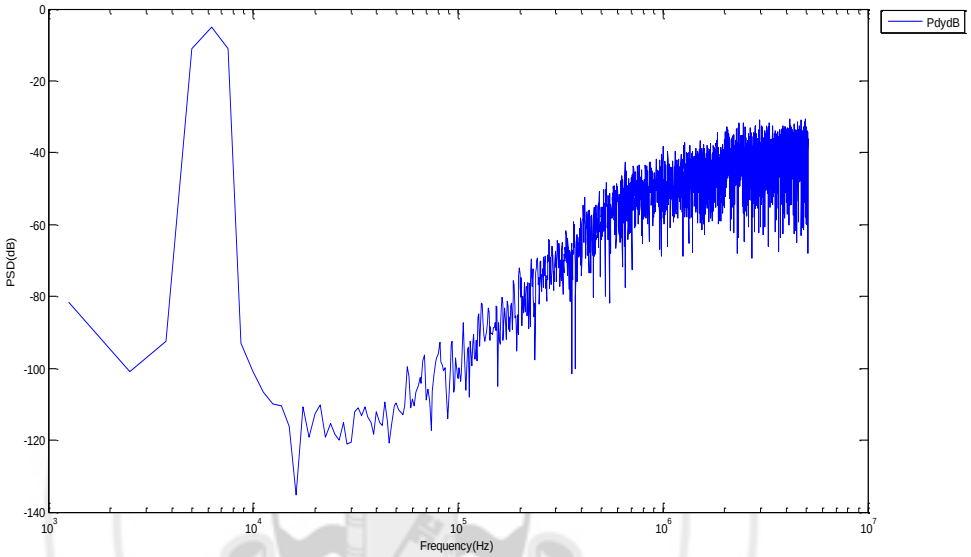



Figure 77 Output PSD for the system

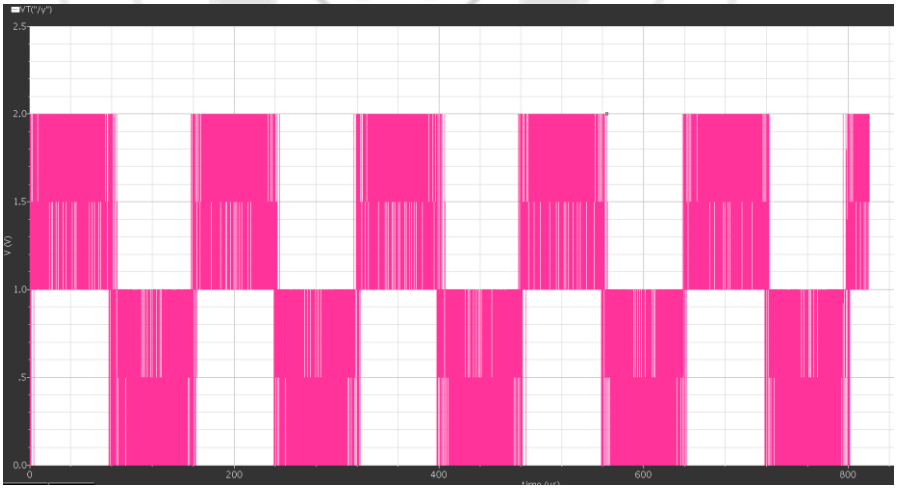


Figure 78 Output waveform

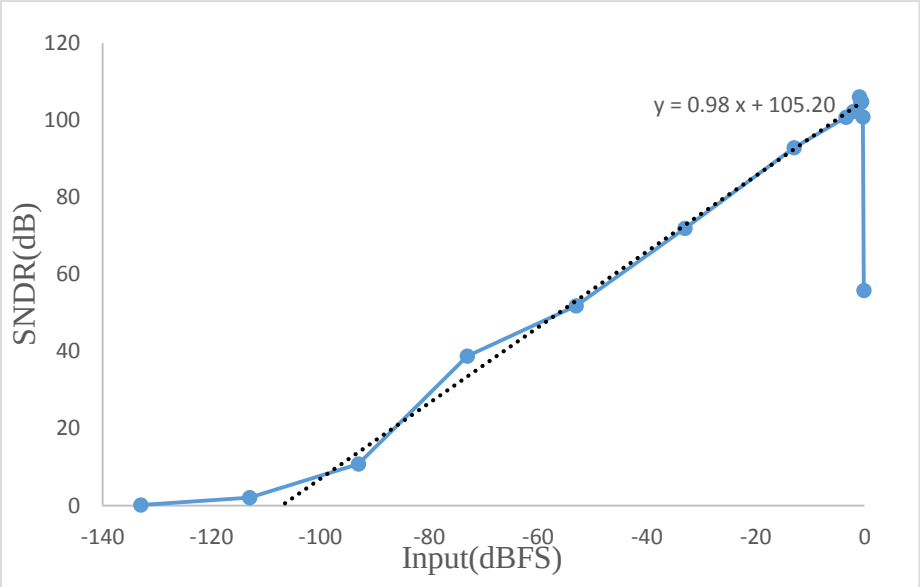



Figure 79 Measured SNDR versus input amplitude

**Power consumption**

For the whole system, the power mainly drive by the op-amps. It can be seen from the table 22 that the first op-amp costs the half of the total power even using the charge pump technique.

Figure-of-merit (FOM) is a character of the system to indicate the relationship between power consumption and the SNDR as well as bandwidth of the system. In other word, it is a efficiency indicator of the system. FOM is defined as

$$\text{FOM} = \frac{Power}{2 \cdot BW \cdot 2^{(SNDR(dB)-1.76)/6.02}} \tag{75}$$

Also, a normal CRFB system is built. The comparison of the system using CP integrator and the conventional one is shown in Table 23. It is seen that with the similar performance, the system using CP integrator as first integrator cost less power than the system using conventional one. It saves around % power by using CP integrator.

Table 22 Power Consumption For Each Part

| part | power |
|---|---|
| 1st Op-amp | 673uW |
| 2nd Op-amp | 338uW |

| | |
|---|---|
| 3rd Op-amp | 321uW |
| comparator | 2*0.02uW |
| total | 1.332mW |
| FOM | 204f |

Table 23 Comparison Of CP And Conventional

| | CP | Conventional |
|---|---|---|
| Technology | 65nmCMOS | 65nmCMOS |
| Sampling Frequency | 10.24MHz | 10.24MHz |
| Bandwidth | 20kHz | 20kHz |
| Peak SNDR | 106dB | 102dB |
| Power consumption | 1.332mW | 1.972mW |
| FOM | 204f/conv. | 479f/conv. |

Besides, the comparison of this work and other work with similar input range (≤1.1), OSR (>100) and BW (<24kHz) is shown in Table 24 Performance Comparison With Other Switch Capacitor Sigma Delta ADCs With Large OSR.

Table 24 Performance Comparison With Other Switch Capacitor Sigma Delta ADCs With Large OSR

| | This work | [17] | [25] | [27] | [46] | [30] |
|---|---|---|---|---|---|---|
| Tech [um] | 0.065 | 0.065 | 0.065 | 0.13 | 0.18 | 0.13 |
| Supply [V] | 1.0 | 1.2 | 1.0 | 0.9 | 0.7 | 1.2 |
| Input Range [$V_{pp\text{-}diff}$] | 0.9 | 1.0 | 0.9 | 1.1 | 1.0 | 0.4 |
| OSR | 256 | 300 | 64 | 128 | 100 | 128 |
| BW [kHz] | 20 | 20 | 24 | 24 | 20 | 10 |
| SNDR [dB] | 106 | 95 | 95 | 89 | 81 | 87.8 |
| Power [uW] | 1332 | 2200 | 371 | 1500 | 36 | 148 |
| FOM [pJ/conv.] | 0.204 | 11.2 | 0.17 | 1.36 | 0.098 | 0.369 |

From Table 24, it can be seen that the FOM performance of this work is better than others except [46] which is inverter-base system. It use pseudo-differential inverters instead of the op-amp to build the integrator, it has high power efficiency but low resolution. And for the [25], it makes use of a special op-amp structure and special local feed-forward structure to get a high power efficiency. For this work, it has higher resolution performance with acceptable power efficiency.

# VIII CONCLUSION

In this project, for audio application, a 3rd order CRFB (*Cascade of Resonators with Distributed Feedback*) sigma delta analog to digital converter with Charge-pump integrator and 1.5 bit quantizer is designed to achieve the target (SNDR≥105dB) set after product survey. Since the high resolution is required in a low bandwidth, a 3rd order sigma-delta modulator with a high OSR (256) is chosen. 1.5 bit quantizer is chosen because it has the advantages of multi-bit quantizer but doesn't affect the linearity of the DAC. After the comparison and simulation in Matlab, the CRFB architecture is chosen for its high SNDR, acceptable integrator input swing and simple adder. Moreover, based on the simulation in Matlab, the behavioral model of the system is obtained, which determines the DC gain, GBW and the slew-rate requirement of the op-amp of the integrators. After that, the circuit is designed in Cadence with 65nm CMOS technology. To implement the integrator and passive adder, the switch capacitor technique is used. And since the first integrator is power hungry, a special integrator called Charge-pump integrator which costs the less power than the conventional one is chosen. For the op-amp design, the different structure chosen because of the different requirement. And for the 1.5 bit quantizer, it makes use of the switch capacitor to compare the input of the quantizer with the reference voltage. Finally, NMOS switch, PMOS switch, CMOS switch and bootstrap switch are used according to linearity of each switch.

As a result (Table 25), with a full-scale input of 900mVpp differential the CRFB ADC using charge-pump integrator achieves 106 dB SNDR and 107dB dynamic range in audio bandwidth (20kHz), while consuming 1.332mW power.

Table 25 The Performance of System

| | Performance |
|---|---|
| Technology | 65nmCMOS |
| Sampling Frequency | 10.24MHz |
| Bandwidth | 20kHz |
| Peak SNDR | 106dB |
| Dynamic Range | 107dB |
| Power consumption | 1.332mW |

| | |
|---|---|
| FOM | 204f/conv. |

**Future work**

From this project, this sigma delta ADC provides a selection for audio applications. So, its performance would be progressively significant in the further. Here it is given a brief blueprint for the future work in the next level study.

Considering the further requirement of energy-saving, the supply voltage would be decreased, so the low power low voltage performance would be the main research issue. In detail, the operational transconductance amplifier (OTA) is the bottleneck for reducing the power dissipation. Circuits could be used in schematic to remove the need for OTAs, or even replacing the OTA with other structures like inverter. Take an overview from system level, because of the stability consideration, some high-order structures could be built in the circuit level in further project. Moreover, for improving the performance, some extra ideas could be constructed like Op-amp sharing technique, which performs noise shaping with only one Op-amp, also very suitable for low–voltage environment; Double-sampling Switch, which samples both phases, thus doubles the OSR with the same power consumption;

Last but not least, continuous time sigma delta ADC, which has become a hot research area, bringing the implicit anti-aliasing filter. It offers unique features that greatly reduce the challenges of deploying ADCs in high-performance systems with high power-efficiency.

All in all, the studies carry on to fulfill the requirements of fast technical development. Those architectures could be our future targets which could be combined with this current work.

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